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## Wafer-level Packaging of Image Sensors

By Giles Humpston

### **Executive Overview**

Each year, several billion CMOS image sensors are manufactured to meet the growing demand for cameras in electronics products, notably camera phones, laptops (web cams) and now TVs. Fabricating device packages at the wafer-level provides economic advantage over discrete approaches since the materials and process costs are shared among the good die on the wafer, which can number many thousands for small die. Wafer-level packages also have the technical advantages of smaller dimensions, shorter interconnects and more consistent part-to-part performance. This article discusses the use of wafer-level packages, which satisfy the requirements.

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Wafer-level packages for image sensors are unique on three counts. First is that the package must have an optically transparent window to permit light from the scene being imaged to reach the sensor. Second, the package has to provide environmental protection to the die in the form of stopping dust and dirt falling on the optically sensitive area. Third, image sensors can be made in two orientations, namely front-side illuminated and back-side illuminated, yet the same package is required to be compatible with both. Meeting these requirements has led to the development of highly specialized, yet extraordinarily low cost, wafer-level packages for image sensors. It is predicted that by 2012 more than 70% of the image sensors produced annually will be housed in wafer-level packages.

### **Semiconductor device packaging**

The traditional functions of a semiconductor device package are to protect the die from degradation by the atmosphere and fan-out the electrical interconnects to the next level. Because of the benign environment in which most modern semiconductors are used coupled with short expected life through product obsolescence, the need for the package to provide environmental protection has virtually disappeared. It is by no means uncommon to see essentially package-less chips attached to circuit boards, with just a polymer covering over the exposed bond pads. However, most semiconductor die are destined to interface to a printed circuit board (PCB) on which the pad size and pitch are fixed by standard, and hence, the package still has to provide the functions of redistribution and fan-out. For die larger than about 5mm on a side, it is also considered prudent for the package to incorporate a laterally compliant layer as part of the interconnect structure to act as a strain buffer. Because silicon has very low thermal expansivity, compared with common (PCB) materials, this layer works to confer acceptable fatigue life on the solder joints of the ball grid array that joins the package to the PCB.

Fabricating device packages at the wafer level provides economic advantage over discrete approaches since the materials and process costs are shared among the good die on the wafer. The benefit is most apparent when die are small and the wafers large so that many thousands or even tens of thousands can be processed simultaneously. Wafer-level packages also have the technical advantages of small footprint, the die and package having the same plan area; shorter interconnects, which permit faster operation/reduced power consumption; and more consistent part-to-part performance, reducing the need for test binning. Despite all of these benefits, development of wafer-level packages acceptable to industry has proved to be challenging and the majority of semiconductor devices are still housed in discrete packages.

### **Solid-state imagers**

There are two principal types of solid-state image sensor, namely charge-coupled devices (CCD) and CMOS. CMOS imagers are able to function both optically and electronically, allowing for reduced size, lower power consumption and simplified assembly. Consequently, CMOS now dominates solid-state imager technology, except for niche applications where optical performance or imager resolution is paramount. Today, image sensor die are manufactured by many semiconductor companies. The smallest standardized area imager is the quarter common intermediate format (QCIF), with a resolution of 25,344 pixels, while the largest commercially available imager has 111 Mpixels.

Solid-state camera modules remained a relatively specialized product until 2001 when a common intermediate format (CIF) camera debuted on a mobile phone. Within eight years, the number of image sensors produced annually went from thousands to over 1 billion. It is estimated that in 2010, more than 80% of all mobile phones will have at least one camera, many having two. Other applications that use solid-state cameras include digital still cameras (DSC), camcorders, automotive driver aids, video security systems, web cams and increasingly, TVs. Together, these applications could consume an additional 1 billion camera modules per year by 2015.

The requirements of a package for a solid-state image sensor are not especially different from other semiconductor devices; the core needs remain a modicum of protection from the environment, redistribution and fan-out of the electrical interconnects, and absorption of thermal expansion mismatch. However, image sensors have one other requirement of the package, namely it must contain a transparent window to permit light to reach the optically active area of the die. The package must therefore contain a glass window – optically "transparent" polymers attenuate too much of the blue spectrum to be useful.

Early solid state imagers were housed in ceramic packages that were closed by a quartz cover slip. This solution, while perfectly functional, is wholly inadequate for high-volume manufacture and applications where the product cost and size are critical. Particular effort was therefore devoted to developing wafer-level packages for CMOS image sensors. This endeavor proved

successful and it is predicted that by 2012, more than 70% of the image sensors produced annually will be housed in wafer-level packages.

### Wafer-level image sensor package

A wafer-level package for an image sensor is relatively simple in concept (**Fig. 1**). A glass wafer is bonded to the front face of the die. Pathways are then formed to connect the die bond pads to a ball grid array interface on the underside of the package. Dicing frees individually packaged die. In reality, the structure and processes are considerably more complex.

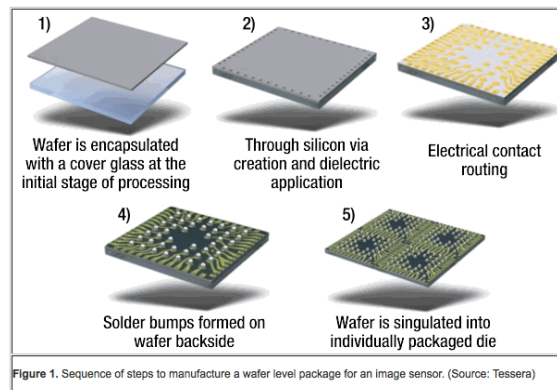
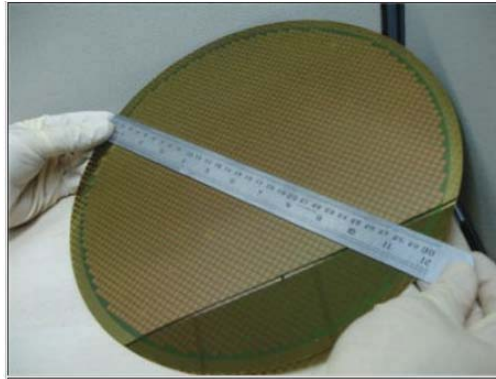


Figure 1. Sequence of steps to manufacture a wafer level package for an image sensor. (Source: Tessera)

The first nuance is the glass wafer itself, which must be expansion-matched to silicon, extremely flat, thin, and free of even microscopic defects since it resides very close to the focal plane of the camera. It must also be available in conformance with SEMI standards. Few companies are able to make glass to the required specifications.

The second detail is that the glass wafer cannot be bonded to the surface of the silicon wafer. This is because the optically active area of the imager is covered with an array of microscopic lenses, one per pixel and typically 1-2 $\mu\text{m}$  high. These micro lenses are very fragile and cannot be cleaned. Any particle of dirt that lands on the micro lens array will stick, due to electrostatic attraction, blocking the incident light and causing a black spot in the image. The solution adopted is to form a picture frame around the micro lens array so that the glass wafer forms an optically transparent cover over the critical area. By attaching the glass wafer as the very first step in the packaging process, micro lenses are protected in their sealed cavity and any contamination that lands on the exterior surface of the glass can be easily removed.

While the glass cover provides protection to the micro lenses, it prohibits access to the die bond pads, which are rendered inaccessible beneath it. To contact the bond pads, some form of through-silicon via (TSV) must be employed. Despite being technically possible for over 30 years, TSVs have never been adopted in high-volume manufacturing. There are many contributory reasons for this, but they all adversely impact either cost, or reliability.



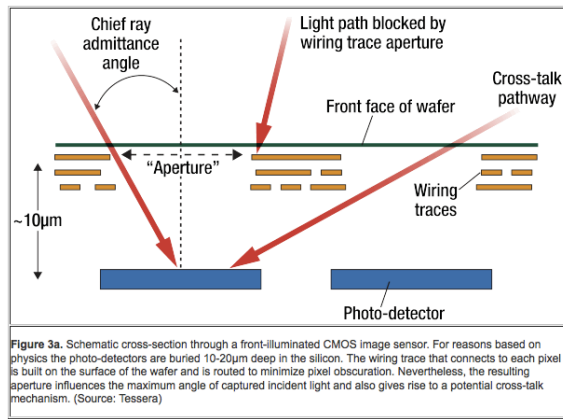
**Figure 2.** 300mm wafer and inset, single imager die housed in a wafer-scale package that uses a via-through-pad interconnect to join the die bond pads to the package lands and from there to the ball grid array interface. The interconnect is based on polymer technology with a single redistribution layer for the wiring trace. (Source: Tessera)

In contrast to most semiconductor die, image sensors have very low I/O counts for the die area. The die bond pads therefore tend to be large and widely spaced to aid process yield. By compromising on the complexity of the I/O redistribution carried by the package, it is possible to fabricate through-silicon vias based on polymer technology with a single metal layer for the wiring trace. This approach helps keep cost low and published reliability data show the package is suitable not just for portable electronics products, but able to surpass the far more exacting automotive reliability standard. A modern wafer-scale package for image sensors is shown in **Fig. 2**.

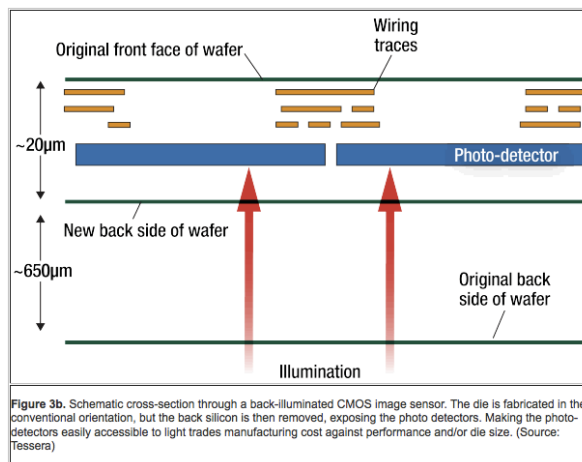
Sighting the TSVs over the bond pads means there are few restrictions on the bond pad size, pitch, or location. The dicing lanes can be as narrow as the silicon design rules allow, which helps to maximize the number of die per wafer and decrease unit cost. The total imager package imager thickness is approximately 500 $\mu\text{m}$ , making it imminently suitable for electronics products where the current fashion is for extreme thinness.

### **Back-illuminated image sensors**

The vast majority of image sensors are front-side illuminated. That is, the light from the scene to be imaged falls on the processed face of the semiconductor, which is also the face on which the die bond pads are sited. Image sensors also come in another flavor, namely back-side illuminated, where the die is mounted inverted and the light falls on the unprocessed face of the semiconductor. This configuration yields superior performance in terms of quantum efficiency and reduced optical cross-talk, together with a reduction in the size of the corresponding camera module (Figs. 3a,b). The principal drawback of back-illuminated image sensors is higher manufacturing cost because additional and more complex processing is required. Hitherto, back-side illuminated image sensors tended to be reserved for scientific and aerospace applications.



Recently, several companies have achieved breakthroughs in semiconductor processing that make back-illuminated image sensors possible for higher resolution imagers on mobile platforms where the attributes of high pixel count, good light sensitivity, and low camera module height are prized. However, the OEMs that integrate image sensors into their products do not want the problem and cost of a different style of package for each imager orientation. Back-illuminated imagers must therefore somehow be fit in wafer-level packages that have the same external structure as packages for front-illuminated imagers.



Visible light is only able to penetrate a short distance into silicon. Therefore, in a back-illuminated imager, for photons to reach the photodiodes, the majority of the original wafer thickness must be removed. Clearly, there are basic handling and yield issues with 200mm or 300mm diameter silicon wafers that have been thinned to under 20µm. Mechanical support is provided by bonding a mechanical-grade silicon wafer to the original front face of the imager wafer. Back-illuminated imagers also use micro lens arrays, so a glass wafer, with closed cavities, is bonded to the light-sensitive side (the back side) of the device wafer. Thus, the bond pads are once again rendered inaccessible for wire bonding, being buried in the center of the glass-silicon-silicon sandwich. The solution is to use TSV technology to access the bond pads. In this instance, the silicon through which the vias pass is the mechanical support wafer. Some subtle process changes are required to fabricate reliable interconnects to the bond pads on a back-illuminated die because of their inverted orientation. The net result is that the imager package can be made

externally identical and the camera module manufacturer does not need to know whether it contains a front- or back-illuminated imager.

The better light sensitivity of back-illuminated image sensors can be put to a number of uses. One of these is to make the pixels, and thus the die smaller, since light-gathering ability is a function of the pixel area. Boosting the quantum efficiency from 25% to 70% permits the pixel size to be reduced from 2.6–1.5 $\mu\text{m}$  per side. For a VGA imager, this permits a wafer to accommodate around three times as many die—a reduction in unit cost that goes a long way toward offsetting the higher manufacturing and packaging cost of back-illuminated imagers.

### **Wafer-level package cost**

Information on wafer-level package cost is difficult to obtain. However, one of the leading camera phone OEMs has published a target procurement cost for camera modules of \$1 per megapixel. For a VGA camera, this means that only a few tens of cents are available to purchase a silicon die, two lenses, an infra-red filter, a light baffle and a housing for the optics, then assemble, test and ship the camera. The wafer-level package is also part of the bill of materials of the camera module, which implies that, to be in contention, the package cost per die must be extraordinarily low.

### **Biography**

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