February 1, 2011

HDI Solution for Very Fine Pitch Flip-Chip Applications

By Vern Solberg

Athough flip-chip assembly is widely accepted in the industry for a broad number of applications, the higher I/O and extremely fine-pitch contact spacing required for newer high-end processor semiconductors have increased assembly process yield challenges. A key concern is how to ensure consistent die-to-substrate interface; a critical barrier in achieving optimum assembly process yield. Historically, the perimeter bumped flip- chip process has served as the main interconnect method in direct-die flip- chip attachment. However, current generations of high density sub-micron wafer fabrication processes are enabling more functionality within the confines of a relatively small die. The smaller die outline forces the semiconductor company to further reduce wire-bond pitch, and it is not uncommon for these higher pin count die elements to be furnished with perimeter-located wire-bond site spacing less than 100µm.

Contact Redistribution

To overcome flip-chip mounting and circuit routing difficulties, companies are relying more on contact redistribution. The redistribution process is performed while the semiconductor remains in the wafer level format and is quite complex. The wafer is prepared using a surface metallization process. A photo-imageable film is then applied and developed to define the circuit pattern for subsequent copper plating processes. When the plating is complete, the copper conductors connect the perimeter wire-bond features to the newly defined contact sites on the die face (typically arranged in a column and row configured array). After chemically etching away the remaining base metallization, the copper conductors are coated with a photo-imaged resist material. Only the array contact sites a left free of the resist coating to enable solder bumping or solder ball attachment. In regard to the solder bumping process, deposition of solder paste at the die contact sites is a common practice, but the process is plagued with control variables. For example, the solder paste material, whether deposited or printed onto the wafer, comprises both solid alloy particles and flux. The ratio of solids to flux can vary somewhat, causing slight differences in the solder bump height when reflowed. Electroplating solder alloy on the contact sites offers significantly tighter tolerance control; however, electro- plating is a slower process than

printing and the plating thickness may not be uniform on all areas of the wafer. As a result, when reflowed to form the bump profile, the bump height can vary by several microns from one die to another.

Although the solder bumping process on the wafer is fairly uniform, precise control of the planarity (common height) of all contact features is not possible. Due to these surface irregularities and planarity issues, a reliable, defect free soldering process remains a viable challenge. The concern is the uneven profile height of solder bumped contact features. A non-uniform bump profile can compromise the integrity of solder interface between the die and substrate. This issue has become even more of a concern for larger die elements having several thousand contacts. Some companies have resorted to a more complex (and rather lengthy) proprietary wafer-level plating process that actually furnishes a raised solid copper post features at each contact site. Although the additive copper plating thickness will not be perfectly uniform across the wafers surface, the Cu post can be made planer by mechanical leveling. Examples for three common flip-chip contact variations noted are compared in Figure 1.

Figure 1. Comparing wafer level applied contact features developed for flip-chip die attachment.

HDI Substrate Development

The most common high density interconnect (HDI) substrate fabrication process used for facilitating high-pin- count direct flip-chip attachment begins with a high grade laminated glass reinforced epoxy-resin core structure. A number of dielectric and copper circuit layers are generally ‘built-up’ onto both sides of the ‘core’ structure using conventional lamination processes. In regard to substrate material, the majority of multi-layer substrates developed for flip-chip packaging rely on one of the commercial high-grade glass-reinforced epoxy compositions (FR-4, FR-5 and B-T). There are also a number of specialty dielectrics that may be required for specific applications. Although developers of these HDI substrates make a strong effort to furnish a balanced structure, substrate warp during the solder joining process continues to be a problem. To overcome the warping effects and other assembly related defects, substrate fabricators are working closely with their customers to explore viable solutions.

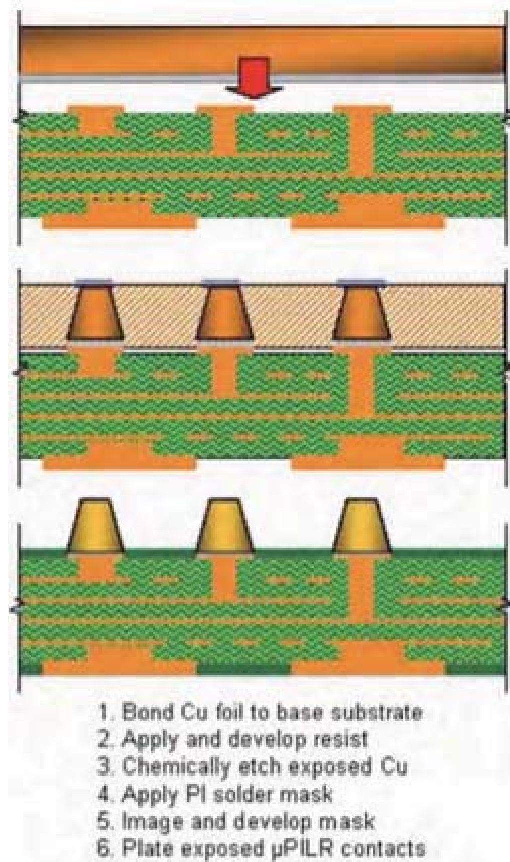

Figure 2. Basic HDI µPILR substrate fabrication sequence.

One solution gaining notice is the µPILRTM, a unique process developed by Tessera. This process furnishes a raised solid copper pillar-like feature at each contact site (Figure 2). The µPILR process requires only slight changes to the basic substrate build-up fabrication methodology. Following the normal sequential fabrication process, a single layer of rolled copper foil is thermally bonded onto the array pattern side of the substrate using standard laminate press systems and a proprietary Cu-Sn-Cu joining process. The example furnished in Figure 3 is a cross-section showing the resulting metallic interface of the µPILR contact and land pattern on a HDI substrate interposer. After completing the bonding process, a photo-resist material is applied over the copper foil, exposed and developed to define the flip-chip array contact pattern. The uncoated copper is then removed using standard chemical etching. The remaining process steps include the application of the photo-imaged solder mask and subsequent Ni/ Au plating of the exposed raised copper features to provide the flip-chip solder attachment methodology. The Ni/Au alloy combination has proven ideal for both eutectic and Pb-free solder attachment of the flip-chip die elements.

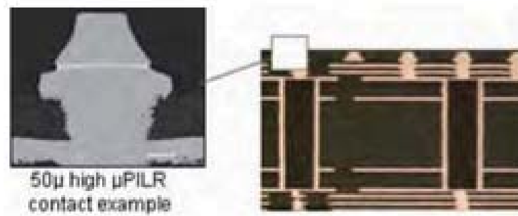

Figure 3. The 50mm-high μPILR contact joined to a very fine pitch land grid array on the HDI substrates top surface.

Flip-Chip to μPILR Assembly Process

During the package development phase of the flip-chip-on-μPILR program, a test die and substrate vehicle was prepared to represent a model currently produced by a leading semiconductor company. The die-to-substrate assembly process begins with the transfer of the alloy bumped die element from its carrier tray or wafer carrier to a shallow flux reservoir. A precise level of the flux is maintained in the reservoir so that only the lower half of the bump contact is actually coated. Although standard die- attach systems can be used for die placement, there are also a number of commercial SMT assembly systems that have the accuracy needed for flip-chip placement. In anticipation of use for flip- chip assembly, these commercial SMT systems also furnish dip-tray stations between the semiconductor pick-up location and the substrate. Figure 4 shows the basic assembly sequence for mounting the bumped flip-chip die onto a μPILR configured substrate. After mounting the flux-coated die, the substrate is transferred to a furnace system to complete the joining process. The temperature and thermal profile developed for reflow solder is dependent on the bump alloy selected. The solder alloy bump provided on the flip-chip test model was a SAC305 alloy composition. While the SnPb eutectic alloy may reach only 218o C the Pb-free SAC alloy generally requires a temperature of 235oC to 245oC to complete the joining process.

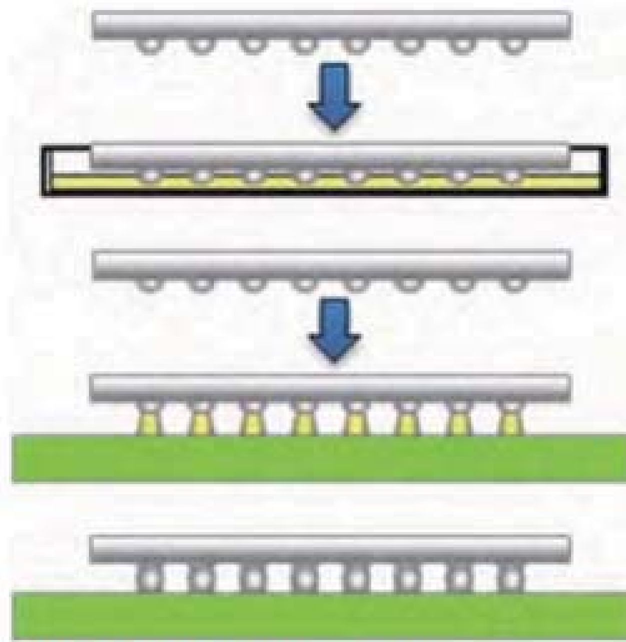

Figure 4. Flip-chip to µPILR assembly sequence.

Post Reflow Reinforcement
How to solve the physical stresses caused by the wide coefficient of thermal expansion (CTE), the mismatch between die (3 ppm/oC) and package substrate (>16 ppm/oC) is a primary challenge facing the packaging specialist. During various operating temperatures, the disparity between the die and the substrate can introduce physical stresses that can compromise the integrity of the solder interface. Traditionally, underfill has been used to decrease the stresses caused by CTE mismatch and to improve solder joint reliability. However, due to the narrow stand-off height and often irregular solder bump profile, uneven flow and voiding in the underfill is common. on the other hand, the uniform standoff height provided by the µPILR contact,enables unrestricted capillary flow of the underfill. Even though the 'tacky flux' material used for initially mounting the bumped die onto the µPILR contact site was rated as 'no-clean', a residue free surface on both die and substrate is vital so that the underfill material is able to flow smoothly and evenly between the surfaces. Figure 5 shows a daisy-chain-configured test die and substrate developed to replicate the physical outline and contact pattern of a functional semiconductor model. The vehicle developed for flip-chip-on-µPILR evaluation included a face- down 20mm x 18mm x 1.75 mm thick, 10,132 I/O solder bumped die mounted onto a 40mm x 40mm x 1.25mm thick µPILR array configured substrate. Key concerns when selecting underfill products are the materials-glass transition temperature (Tg) and CTE after curing. In addition to the Tg and CTE issues, the underfill material selected needs to provide process uniformity and ensure end-product reliability.

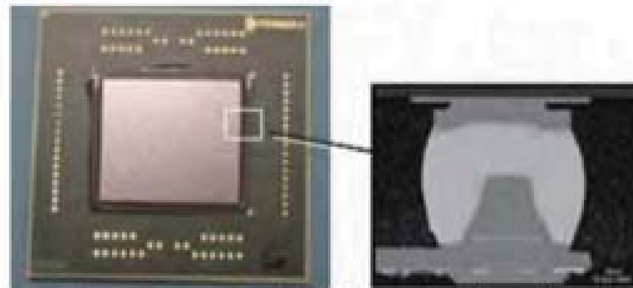

Figure 5. Post underfill example of a reflow soldered 10,132 I/O bumped flip-chip semiconductor mounted onto a µPILR substrate.

Final Assembly Process

Following the basic flip-chip assembly and underfill process, pre-formed solder alloy spheres are attached to the bottom side of the substrate. The process used for attaching the solder spheres to the bottom surface of the package begins with a stencil printing process that deposits a thin layer of ‘tacky flux’ at each contact site. Following solder ball placement, the flip-chip assembly is transferred once again to a reflow soldering system to complete the joining process. The systems commonly used for thermal reflow attachment of the solder spheres is a conveyor type, multiple zone convection oven. Time and temperature parameters for reflow soldering are closely monitored. The thermal profile developed for solder- ball attachment for the µPILR test model established an overall time duration of approximately 60 seconds above liquidus with a peak temperature of 240oC. The reflow procedure was followed by a dynamic cleaning process using an alcohol/water solution to remove any surface residue. Following electrical testing, X-ray, and visual inspection, a coined copper alloy heat spreader was mounted onto the top surface of the package. The final assembly step was the bonding of a heat spreader to the semiconductor back surface and the substrates perimeter edge area (Figure 6). This was achieved using a relatively low melting temperature Indium alloy as the thermal interface material (TIM) and a low modulus polymer compound for edge sealant.

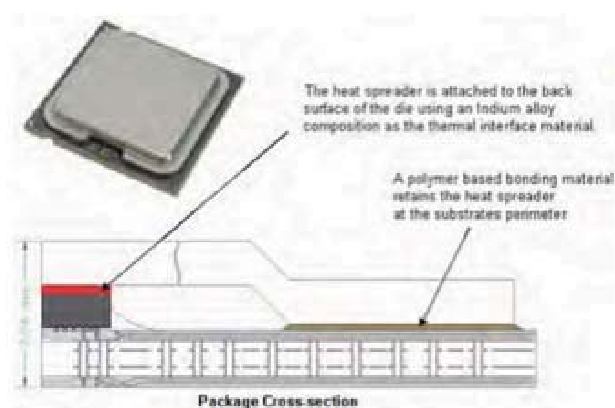

Figure 6. Heat spreader attachment.

Conclusion

The µPILR technology has proved to be a truly novel approach for flip-chip substrate fabrication. The raised contact format is proving to be a practical low- cost solution for the finer-pitch flip-chip applications because it overcomes most of the assembly process yield concerns. This is due to the precise standoff height and the slightly tapered profile of the solid copper contacts. The small diameter contact profile not only enables finer contact pitch but it accommodates higher density circuit routing. Because the copper foil is furnished with a uniform thickness, a near perfect planer surface is retained for mounting the solder bumped flip-chip die. Soldering the flip- chip die onto the µPILR contact has also proven to furnish a physically stronger die-to-substrate interface and a more uniform standoff profile when compared to common bumped flip-chip-on-land and copper-post-on-die technologies.

Acknowledgements

Key contributors in the preparation of this article included Tessera's Ilyas Mohammed, Ellis Chow and Laura Mirkarimi. Note: µPILR is a trademark of Tessera Inc. or its affiliated companies in the United States and other countries.

http://issuu.com/chipscalereview/docs/csr_jan-feb-2011_digital/