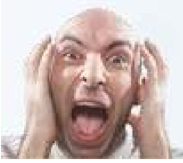
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[Leapfrog: First Look]

Back-Illuminated CMOS Imagers May Increase Cell-Phone Camera Sensitivity By Two F-Stops

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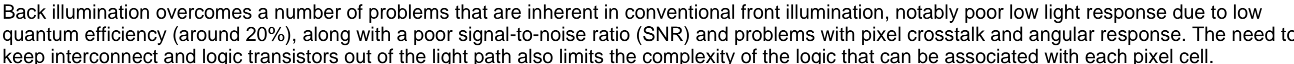
Reprints

Tessera Technologies reports a conflict (and resolution) between the need to reduce cell-phone imager chip cost and size by producing everhigher-resolution imagers on smaller die and the consumer demand for digital-camera image quality in cell phones. The most recent solutions separate image capture from image processing—in other words, moving that processing, which can be accomplished using relatively cheap CMOS, off the more expensive imager chip.

The greater flexibility this permits recently led to some imager innovation by Sony and other companies. One key aspect to their developments is whether the imager is arranged so the light from the scene being photographed strikes the pixel sensors on the imager array from the front or the back of the die. Back illumination has some significant advantages.

Essentially, back illumination is a bonded wafer process in which the imager wafer is thinned from the back side until the photodiode array is very close to the surface, flipped, and bonded to a second wafer that provides rigidity. Taking away the topside thickness needed for the metallization layers causes light to travel a shorter distance through the silicon to reach each pixel photodiode (*see the figure*).



Back illumination overcomes a number of problems that are inherent in conventional front illumination, notably poor low light response due to low quantum efficiency (around 20%), along with a poor signal-to-noise ratio (SNR) and problems with pixel crosstalk and angular response. The need to keep interconnect and logic transistors out of the light path also limits the complexity of the logic that can be associated with each pixel cell.

In contrast, back illumination provides quantum efficiency on the order of 80% and superior optical properties, due to the shorter distance light must travel through the silicon to reach the pixel. The pixel processing logic is on a separate, purely CMOS chip, so it can be as sophisticated as necessary. The downside is fabrication cost. Lapping and bonding add manufacturing steps, and the support wafer blocks access to the bond pads on the active wafer.

WHAT'S NEXT?

Tessera estimates that even allowing for economics of scale (more die per wafer), mass-produced back-illuminated die will cost twice to four times as much as front-illuminated die with similar resolution. Yet the payoff is what is estimated as five times improvement in performance overall. Sony, for example, claims a gain of 8 dB in sensitivity, with 6 dB of that due to better quantum efficiency and 2 dB due to lower SNR. So, back illumination is taking off.

Working with Taiwan Semiconductor Manufacturing Corp. (TSMC), OmniVision believes it has found the key with its OmniBSI approach (see *"CMOS And CCD Image Sensor Breakthroughs Promise A 'Bright' Future*). The company can produce 8-Mpixel devices from a 1.4-µm process for mobile phones.

Sony has also seen success with backside illumination. It has produced a 5-Mpixel device on a 1.75-µm process for mobile phones, digital cameras, and camcorders. And STMicroelectronics, working with CEA Leti and TraciT Technologies, has demonstrated the feasibility of manufacturing 3-Mpixel CMOS imagers on a 1.45-µm process using backside illumination.

Tessera's interest in back illumination lies partly in licensing its own imaging technologies, such as its OptiML wafer-level optics, and partly in the packaging. The company estimates that OptiML can extract a further f-stop in light gain over that achievable by back illumination, eliminating the need for flash in many lighting situations. Additionally, its Shellcase micro via pad (MVP) technology deals with the support-wafer problem and facilitates die stacking. **DON TUITE**

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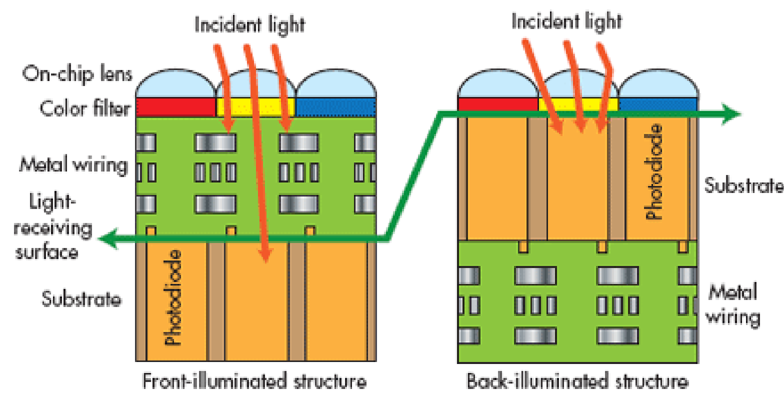
fig 1



Backside illumination flips the imager wafer, lapping it until the photodiode array is close to the surface, and bonds it to a support wafer before wafer-scale packaging and singulating the individual imagers. The results are much higher quantum efficiency (output per photon), lower SNR, and a wider acceptance angle for incident light.

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