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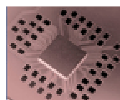

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Packaging Challenges in High Performance Computing

Introduction

Ilyes_Mohammed

Over the past half century, the semiconductor industry has been at the forefront of technological progress as demonstrated by its own products and what they have made possible.

The main areas of improvement include functionality per unit volume, speed of performance, power consumed per unit performance, cost per function, etc. The bulk of the credit goes to the miniaturization and integration at the chip/wafer level as predicted by Moore's Law, and made possible through advancements in manufacturing, design, simulation and materials.

Even less than twenty years back, packaging was considered an afterthought by most of the industry, though the high performance computing segment was the first to devote significant resources for optimizing the package performance.

Starting with the C4 flip-chip package, there have been steady improvements in high performance packaging including having interconnects greater than 10,000, pitch less than 200 μm, migration from ceramic to organic substrates, and from high-lead to lead-free interconnects. But fundamental challenges remain, and the ones that impact packaging are:

(i) cost-effective manufacturing with interconnects at finer pitch than 150 μm,

(ii) mitigating the failures induced by high currents due to the phenomenon termed electromigration,

(iii) reliability of low-k dielectrics and interconnects under thermo-mechanical loads, and

(iv) materials and assembly issues. The industry is addressing these issues through

(i) substrate development including solder on pad application improvements,

(ii) interconnect modifications to avoid Copper depletion and creation of voids,

(iii) optimizing the underfill properties to balance the stresses in the low-k dielectric and interconnects, and

(iv) underfill process improvements using jet or vacuum dispense.

The one feature that has the most impact on the above mentioned issues is the interconnect structure. The current ones in the industry include high-lead solder bump, lead-free bump, copper core, copper post, etc.

In this article, an interconnect structure called μPILR^{TM} interconnect is presented in detail as it addresses each of the four challenges identified above. It consists of a substrate manufacturing technique that results in a

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copper structure on a substrate pad. This eliminates the need for applying solder on substrate, which is an issue at finer pitches.

Due to the presence of copper structure, the failure due to electromigration phenomenon is significantly delayed on the substrate side due to the fact that there is enough copper to eventually form a relatively stable intermetallic, which has much lower migration rate compared to copper in tin. This retards the void growth and hence improves reliability.

Due to the 3D nature of the µPILR interconnect, the aspect ratio (height to diameter) is higher than a solder bump; which eases the package assembly issues such as interconnect joints yield, underfill voids, etc.

Finally, the reliability is improved because the fracture toughness of the µPILR interconnect is higher than solder bump as the µPILR structure acts as a fatigue crack growth inhibiter. It also offers better low-k dielectric reliability as the lead-free solder interface on the chip side exerts lower stress than the copper post on chip. This article presents design, simulation, substrate manufacturing, package assembly, electromigration and reliability results for a test vehicle representing CPU applications.

Flip-chip Interconnects

There are three main types of flip-chip interconnect being used in the industry: high-lead bump, lead-free bump and copper post. These three types are shown in Figure 1. The high-lead bump is being phased out due to ROHS requirements. The lead-free bump has fine-pitch limitations due to solder collapse and has low electromigration performance.

The copper post is emerging as an option for high performance packaging as it offers fine pitch capabilities and has good electromigration performance. Some of the issues with copper post on chip are lower reliability with extreme low-k dielectrics and relatively higher cost. In this paper, a new type of flip-chip interconnect called µPILR is presented that offers the advantages of copper post on chip (fine pitch and good electromigration performance) while offering good reliability and lower cost.

The typical failure modes seen in interconnects are shown in Figure 2. They are related to interconnect reliability (solder joint fatigue life), package reliability (low-k dielectric cracking) and package performance (voiding due to electromigration phenomemon from high current densities).

A new interconnect design has to address these issues while offering a roadmap to fine-pitch well below 100 µm and be able to be manufactured using conventional industry equipment and materials. The µPILR interconnects [1] as shown in Figure 3 consist of an array of solid copper pillars that are part of the substrate.

Depending on the method of manufacturing, these interconnects have different sizes and shapes, and can be joined to chips with or without copper posts. Some of the different configurations are shown in Figure 3.

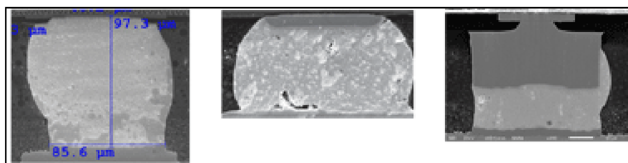


Figure 1: The three common types of flip-chip interconnects in high performance applications are high-lead bump, lead-free bump and copper post

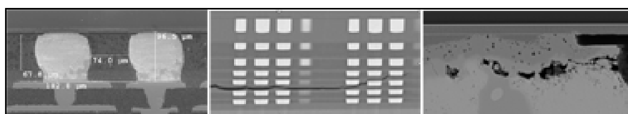


Figure 2: Solder fatigue, low-k dielectric cracking and electromigration voiding are the three main failure mechanisms in high performance flip-chip interconnects

Figure 3: The μPILR interconnect

μPILR substrate

The μPILR substrate can be manufactured with or without laminate core. The coreless method consists of starting with a copper sheet as the base layer, carrying out the build-up process to the required number of layers and then processing the copper sheet to form μPILR interconnects. The core-based substrate approach is shown in Figure 4. It consists of starting with a conventional substrate and then attaching a copper sheet and forming μPILR interconnects. The main technical challenges in this process are:

- Uniformity of joining layer and its surface properties
- Formation of μPILRs through various techniques
- Removing of joining layer and intermetallics without damaging the top circuit layer and
- Uniformity of solder mask and alignment

Figure 5 shows the μPILR interconnects on the substrate. As they are formed from a copper sheet, the measured co-planarity was excellent (± 2 μm). The substrates underwent conventional hot oil tests (20-260 ^{0}C, 50 cycles) successfully. Bump shear tests were done before and after ageing (150 ^{0}C, 1000 hours) and the shear force was in 40-60 gm range, well above the required 35 gm force.

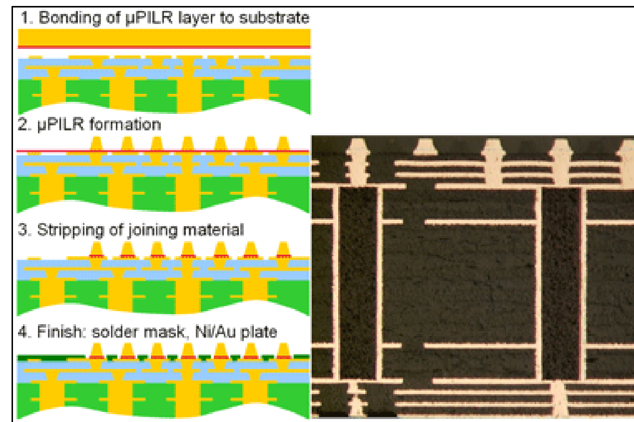


Figure 4: A method of manufacturing μPILR substrate using core-based substrate

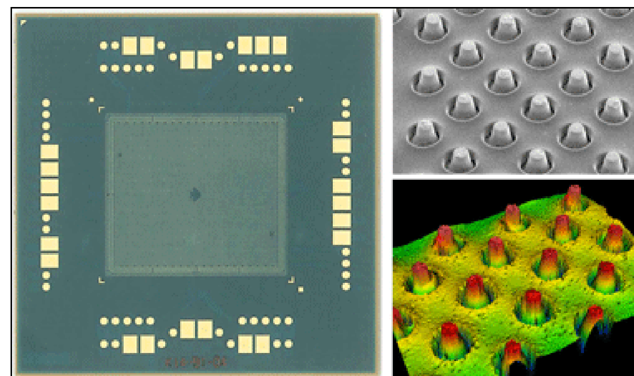
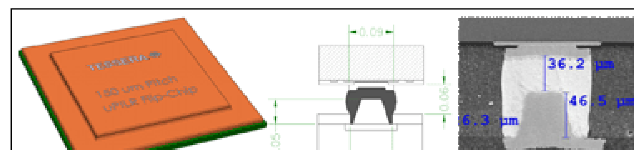


Figure 5: μPILR substrate with interconnects that are highly co-planar



Test vehicle design and assembly

Figure 6: Test vehicle design for reliability and electromigration testing

The test vehicle was designed to represent a high computing application. The chip measured 20 mm x 18 mm x 0.75 mm with 10,132 interconnects at 0.15 mm (signal) and 0.2 mm (power/ground) pitch. The substrate measured 40 mm x 40 mm x 1.2 mm and had 10 metal layers in a 3-4-3 build-up on core stack. The interconnect details along with the package cross-section are given in Figure 6.

The package assembly was done using conventional flip-chip equipment and processes. After process optimization, both flip-chip reflow and underfill processes were close to 100% yield. Figure 7 shows the package assembly results. After the underfill process, the heat spreader was attached with Indium as the thermal interface material (TIM), according to the design as shown in Figure 6.

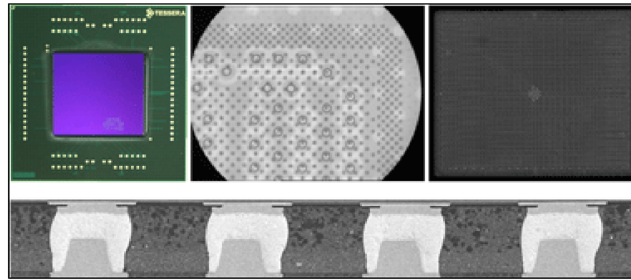


Figure 7: Package assembly results using conventional flip-chip reflow and underfill processes yielded near 100% with well-aligned joints and void-free underfill

Electromigration Performance

For high performance computing, two main requirements are electromigration performance and reliability. The electromigration testing was done under two different conditions. The samples passed 1300 hours without failure under accelerated test conditions of 30.0kA/cm^2 (1.0A) & 160^{0}C and passed 1000 hours without failure under highly accelerated test conditions of 45.0kA/cm^2 (1.5A) & 160^{0}C.

The resistance was monitored continuously and the rise in resistance was less than 3%. The cross-section pictures in Figures 8 and 9 show the results. There are no voids on the substrate side and void formation can be seen on the chip side.

Figure 8: Electromigration testing (1.0A, 160C) sample after 1300 hours

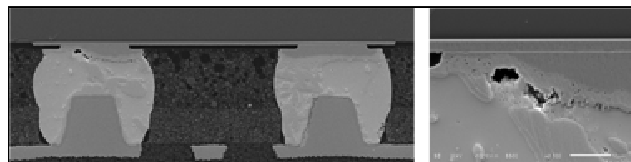


Figure 9: Electromigration results (1.5A, 160C) sample after 1000 hours

Compared to published results for high-lead bump, lead-free bump and copper post on chip [2, 3], these results are the best when the acceleration factors are taken into account. It is estimated that the acceleration factor is approximately 2.5x from 15.0kA/cm^2 to 45.0kA/cm^2, and about 2x from 125^{0}C to 160 ^{0}C for a total of 5x for 45.0kA/cm^2 & 160^{0}C compared to

15.0kA/cm^2 & 125^{0}C test conditions.

This implies that 1000 hours of successful testing under 45.0kA/cm^2 & 160^{0}C corresponds to about 5000 hours under 15.0kA/cm^2 & 125^{0}C, which is better than the results published in [4] for copper posts on chip.

Reliability

The reliability simulations were done comparing the copper post on chip and µPILR interconnects under two test conditions, -55 to 125 ^{0}C (thermal shock) and 0 to 100 ^{0}C (thermal cycling). The results are summarized in Table 1. The µPILR interconnect is expected to pass the reliability tests and is approximately 20% better in fatigue life, which is primarily due to the extra amount of solder.

Reliability testing was also done and no failures were observed after 1000 cycles under -55 to 125 ^{0}C thermal shock test conditions. Figure 10 shows a cross-section of the interconnect after the termination of the test.

Table 1: Fatigue life prediction for the two types of interconnects

Interconnect Type	-55 to 125 ^{0}C		0 to 100 ^{0}C	
	Crack initiation	Characteristic life	Crack initiation	Characteristic life
µPILR	929	1831	2071	3586
Cu post	732	1442	1631	2824

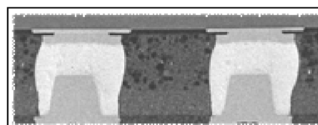


Figure10: µPILR interconnects after 1000 cycles (-55 to 125 0C)

Conclusions

The packaging performance has to keep improving to meet the ITRS roadmaps and to minimize negatively impacting the performance of the chip and the system. The flip-chip interconnects are the key enablers for better package performance through improvements in fine-pitch, current carrying capacity and reliability.

High-lead bumps are being phased out and lead-free bumps have limitations regarding fine-pitch and electromigration performance. Copper post on chip and µPILR on substrate are two interconnect technologies that meet the future packaging requirements, with µPILR expected to perform better in reliability.

The reliability benefit gets more pronounced with the transition from low-k to extreme low-k dielectrics on the chip side. More research work is ongoing with µPILR interconnects and more research in general is needed by the industry to ensure that the packaging for high performance computing facilitates excellent electrical and thermal performance while meeting reliability and cost requirements.

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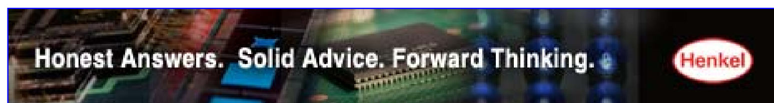

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