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Setting A New Standard For Through-Silicon Via Reliability

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Historically, the speed and complexity of electronic circuits required for manufacturing has out-matched the interconnects used to join circuits together. A first approximation of interconnect performance controls are:

- Power consumption (capacitance, voltage, frequency)
- Signal speed (resistance, inductance, capacitance)
- Signal integrity (inductance, capacitance)

Various strategies have been devised to address these controls. For example, materials and process innovations have led to copper tracks and low-k dielectrics, while novel circuit designs have given rise to the 64-bit-wide bus, multi-data transfers per clock cycle, and synchronous clock technologies.

However, the performance of each interconnect is fundamentally dictated by its length, width, and thickness. Device integration solutions like system-on-a-chip (SoC) and 3D stacking are intended to directly address these controls. In the case of 3D stacking, the objective is to replace the long, horizontal, wiring traces that become necessary when die are placed side-by-side with short, vertical pathways, concomitantly reducing the three fundamental controls of resistance, inductance, and capacitance.

Making vertical interconnects generally requires some form of through-silicon via (TSV) technology. TSVs are conceptually very simple to produce and many variations exist. A common implementation is a hollow pipe with near-vertical sidewalls, machined through the thickness of the silicon. A dielectric film overlaid with conductive metal is applied to the sidewalls of the pipe. Generally, TSVs furnish electrical pathways between bond pads on one face of the die and lands on the opposing face ([Fig. 1](#)).

TSVs aren't new; they have been used on commercial products since 1976. All GaAs die with coplanar RF circuits use through vias to provide grounding points.

However, despite many years of work, TSVs have failed to achieve widespread adoption. There are several reasons for this, including the high cost of the wafer-scale equipment required, the slow etch rate of silicon that curtails throughput, and the complexity of the additional process steps to fabricate conductive pipes that are insulated from the silicon through which they pass.

Furthermore, issues of reliability have yet to be satisfactorily solved. Points of weaknesses in the design include dielectric and conductive coating of the side walls of a high aspect ratio pipe, and the 90 degree bends at the top and base of the pipe that the redistribution layer must traverse and maintain connectivity during thermal cycling. There's also the issue of cleaning the back of the bond pad so that the redistribution layer can make an ohmic contact to it.

Developing a TSV technology that addresses all of the above problems remains elusive. However, by focusing on special-case conditions, it's possible to realize TSV solutions that meet all three requirements for commercial success, namely adequate functionality, low cost, and proven reliability. An example is wafer-level packages for solid-state image sensors.

WLPS FOR SOLID-STATE IMAGE SENSORS

Typically, more than two billion image sensors are produced each year. These are primarily incorporated in portable electronics products such as camera-enabled cell phones, digital still cameras and increasingly, laptop and netbook computers. Like most other semiconductor devices, solid state image sensors require some form of enclosure to ensure longevity. Traditionally, this was achieved using chip-on-board (COB) assembly processes, but the industry is now transitioning to wafer-level packaging (WLP).

A wafer-level cavity package for an image sensor is achieved simply by applying a picture frame of adhesive around each die, attaching a glass wafer, and then sawing the assembly to yield individual die, each with a cover over the delicate image sensor area ([Fig. 2](#)).

WLP has great economic value for image sensors. In WLP, the die are packaged in the wafer while still in wafer form and the wafer is then singulated to free individually packaged die. Thus, the costs of packaging are shared among the good die on the wafer, greatly reducing packaging costs per die. With typically between 750 and 1250 die on a 200-mm-diameter image sensor wafer, this results in an order of magnitude decrease in the packaging time and cost per die, compared with COB assembly.

Furthermore, it's possible to provide wafer-level packaged die with a ball-grid-array (BGA) interface. This allows the camera module to be soldered to the main printed circuit board (PCB) of the product simultaneously with all other semiconductor and passive components, saving on component integration costs.

Forecasts indicate that by 2011 more than 50% of all imagers will be enclosed in a wafer-level package.

WLP TSVs

An imager die must be mounted face-upward so that the optically active area is exposed to the scene of interest. This means the BGA interface must be on the opposing side of the package. Therefore, some form of TSV is required to provide pathways between the bond pads on the die and the package lands. To be commercially successful, these TSVs must meet certain minimum requirements in terms of functionality, cost, and reliability.

Functionality is the easiest specification to meet. Image sensors are mostly designed for end use in portable electronics products where processing speed and power draw is limited. In general terms, this means low megahertz frequencies, potentials below 10 V, and current levels of milliamperes. Virtually all known TSV technologies can deliver the necessary functionality.

The cost of making the TSVs is critical. The very high volume of image sensors required by the camera-phone industry means there's intense pressure on suppliers to decrease component costs. The International Semiconductor Equipment and Materials Consortium has a stated goal to "create a robust integrated process flow...[for a TSV process]... at a total cost of ownership of under \$150." Even though this goal has yet to be achieved, it's simply too expensive for a wafer-level image-sensor package, considering the industry objective is to achieve the sub-\$1 VGA camera module.

The image-sensor package must obviously meet industry specifications for device- and board-level reliability. The vast majority of announcements regarding TSV solutions either fail or decline to publicly disclose product reliability data. From this, it must be concluded that those solutions are wanting in this regard.

The exceptionally high volume demand for wafer-level-packaged imagers affords the luxury of developing a custom TSV solution that can circumvent the limitations of known TSV technology.

VIA-THROUGH-PAD TSVs

A typical modern wafer-level package for image sensors is the Tessera SHELLCASE MVP solution ([Fig. 3](#)). This package design has few restrictions on wafer diameter, bond pad size, pitch or location, making it directly compatible with most existing CMOS imagers. The dicing lanes can be as narrow as allowed by the silicon design rules, which helps to maximize the number of die per wafer and decrease unit cost. The packaged imager thickness is approximately 500 μm , suiting it for electronics products that demand extreme thinness.

The bond pads and lanes of the ball grid array are connected by a via-through-pad TSV. Via-through-pad TSVs have appropriate electrical characteristics for

the application. Taking the worst case of a 3.2-mm-long track on the underside of the package, the entire interconnect from the die bond pad to the land of the solder sphere will have a resistance of 270 m Ω , a capacitance of 0.99 pF, and an inductance of 0.74 nH. The dielectric permittivity and loss of the materials set are perfectly acceptable for the data rates of conventional video cameras, but are unsuitable for frequencies above a few hundred megahertz.

The via-through-pad TSV superficially resembles a conventional TSV, but the differences are important and have profound implications for product cost and reliability. The first difference is that the passageway through the silicon is purely mechanical and needs only to expose some of the area of each bond pad. This permits a relaxation in alignment tolerances and substantial savings in equipment and mask costs. Secondly, the profile of the openings can be relaxed to a trapezoid with rounded corners. This eliminates one of the main sources of unreliability with conventional TSVs.

The third difference is the use of polymer technology for the dielectric, applied in liquid form. This is much less expensive and more reliable than inorganic coatings, which must be applied by expensive vapor-phase process equipment and can be susceptible to catastrophic brittle fracture.

However, the key difference is that the conductive metal of a via-through-pad TSV penetrates through the thickness of the bond pad to form a circumferential edge contact. This is structurally identical to the well-established wafer-level edge contact technology and has the same inherent reliability. Because the act of penetrating the bond pad exposes fresh metal at the circumference, this solution obviates the difficulty of making ohmic contact between the conductive metal of the via and the bond pad, when the bond pad is the closed end of a high aspect ratio pipe. The end result is higher process yield and product reliability.

ACCELERATED RELIABILITY TESTING

Evaluating the reliability of semiconductor packages is a time-consuming process. Many companies use quick screening tests, which typically give a good indication of the likely outcome. Solid-state imagers and MEMS packages that have a sealed cavity can use the following test:

Autoclave: 120°C; 100% RH for 168 hrs; followed immediately by lead-free solder reflow: step heat/cool 25°C to 280°C to 25°C (30 sec dwell) x 20 cycles

Wafer-level cavity packages with via-through-pad TSVs will pass this test.

PACKAGE-LEVEL RELIABILITY

Components intended for integration into products must be applicable for that purpose. Meeting this criterion is usually demonstrated by subjecting batches of component parts to various environmental regimes, which must be survived. For conventional semiconductor parts, these tests are defined by industry standards,

one of the most arduous of which applies to automotive applications. ([Table 1](#)) summarizes the principal package-level tests and accompanying environmental parameters.

A typical test sample comprises a minimum of three lots of 77 parts taken from production batches manufactured on different days, by different shifts, on the full range of equipment available. As can be seen from ([Table 2](#)), imager die protected by wafer-level packages using via-through-pad interconnects exhibit a margin of safety of more than two and often substantially more over the required reliability standards.

BOARD-LEVEL RELIABILITY

The test vehicle selected for this application measured 6 x 7 mm. It was packaged at the wafer-level with via-through-pad TSVs and equipped with a μ BGA interface of 200- μ m-diameter solder balls consisting of SAC305 composition. The chip-scale packages (CSPs) were attached to eight-layer, 1-mm-thick FR4 board having 350- μ m-diameter lands for each solder ball. SAC305 solder paste was used for package attach.

The wafer-level packages measured 600 μ m in thickness. Prior to attachment to the PCB, the packages were pre-conditioned to MSL1. That is, a bake in air at 125°C for 24 hours, followed by a bake in a damp environment at 85°C with 85% relative humidity for 168 hours, and finally exposure to three consecutive thermal excursions, each representative of a lead-free solder reflow cycle.

After attachment to the PCB, the μ BGA interface collapsed slightly, giving a package-to-board spacing of approximately 150 μ m. Underfill material (Namic SUF 1570) is introduced into this gap, which was then cured in accordance with the manufacturers recommendations. A total of 50 parts were manufactured for this trial.

The components were subjected to automotive board-level environmental tests ([Table 3](#)), which included the most aggressive of tests for electronic assemblies, namely cyclic thermal shock. This comprised a dual chamber system, with the cold chamber set at -40°C and the hot chamber at +85°C. The dwell time in each chamber was 5 minutes and the transfer time less than seven seconds.

The results, which are also incorporated in Table 3, show that no failures were recorded at all. In the case of thermal shock, no failures occurred even after testing was extended to 1250 cycles.

CONCLUSION

TSVs can be used to provide circuit-to-circuit and die-to-package interconnects. While many variations of TSVs have been developed over the years, the applications remain limited because of high cost and/or poor reliability.

Via-through-pad TSVs have been engineered for the specific application of wafer-level packages for solid-state imagers. Focusing on one product type has made it possible to engineer a TSV solution that works for a specific application, is very low cost, and extremely reliable. Indeed, the package using via-through-pad TSVs will comfortably pass automotive component- and board-level reliability tests.

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