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The Miniaturization-Integration Balancing Act

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Since its launch in 1990, Tessera has assumed a leading role in next-generation packaging technologies. This month, Craig Mitchell, senior vice president of the company's Interconnect, Components and Materials (ICM) division, himself an inventor on some 32 patents, talks with editor-in-chief Mike Buetow.

CA: Packaging today consumes much of the total cost of the end-product. Does Tessera try to drive end-products through its packaging inventions, or do you take your cues from the form factor?

CM: Traditionally Tessera has focused on chip-scale packaging and multichip modules. Going back to our founding, we recognized the importance of understanding SMT requirements and assembling them to boards. We see continued migration to finer pitch. Some of the pushback is from the impact on the board cost and assembly yields. We are seeing some volume on 0.4 mm pitch and believe we will get to 0.3 mm product late next year in cellphones and some other handheld devices.

Cellphones are a key driver for semiconductor package technology today. Desktop PCs pushed semiconductor package technology from a performance perspective, but now cellphones are pushing it. Consider, one cellphone could have a baseband processor, a multimedia processor, and an application processor. That's three different processors, each with a few hundred I/O to several hundred I/O. It's forcing the industry to come up with ways to evaluate finer pitch because they don't want to increase the [physical] area of a given product.

CA: Does Tessera concentrate on non-handheld markets?

CM: We are concerned with high volume, because we want to help enable our licensees to do high volume. So we focus on a select few markets. Cellphones ship over 1 billion units each year – that's high volume. Notebooks ship about 150 million units, but there could be four to eight DRAMs per notebook, which

drives up unit volume. We develop prototypes and then work with licensees to introduce the technologies.

CA: Do you get pushback on your designs from others in the supply chain?

CM: We do prototype samples and get feedback from board fabricators. We get some feedback [from them] on cost and yield. We are also talking to packaging licensees, who get information back from their customers. And we get feedback from OEMs on cost levers.

CA: What is Tessera's involvement on the various industry roadmaps for packaging?

CM: We have been involved in some of the various roadmaps, such as ITRS and IPC, and try to stay in touch with those. We're not doing anything with iNEMI at this time. Roadmaps are a guide. They are not the gospel, if you will, but a general direction of where the industry is headed.

CA: How do you set your roadmap?

CM: It's through direct involvement with semiconductor manufacturers and OEMs. I think that's the same with many companies. It's the customer that drives us. The intention is to collect information from across the industry and get unbiased info, and to see the issues that people specifically see. But you have to look at what's happening in the industry and how you can best solve your customers' challenges.

CA: Generally, the smaller the form factor, the more thermal management comes into play. How does Tessera factor this in?

CM: Depending on the customer, we may or may not have to do some optimization for thermal management. We look at the various materials, minimizing interconnect lengths, reducing copper content, and trying to reduce overall thermal resistance. We do a fair amount of modeling to try to understand the thermal performance. In the notebook space, Tessera has been developing technology to provide very low profile cooling methods. We call this silent air cooling [technology]. This leverages electro-hydrodynamics, and involves taking an electrode and cathode, applying a voltage across the two, ionizing the air molecules, and adding a charge. The air molecules bump into other molecules and provide airflow without any moving parts.

I think thermal management has to be managed at various levels. You have to look throughout the chain and understand how to balance thermal resistances throughout that chain. It may mean allowing some residual copper on the board in order to spread heat, instead of etching it away.

CA: At what point do you involve the EMS/ODMs?

CM: We give the EMS providers an update on where we see things headed and introduce them to our latest and greatest. For example, our MicroPillar Interconnect technology uses a copper pillar formed during the fabrication process. We talk about the impact on board assembly. We actually go through an evaluation, where we supply a test board and package, and [the EMS company] assembles it and gives us feedback on it. The soldering, placement, reflow, the results and yields, and recommendations on how we might improve design rules, be they package, PCB or substrate design rules.

CA: How often does this take place?

CM: In certain cases it's a standing relationship, maybe a couple times a year. It changes over time. Generally, we try to keep a direct relationship. Sometimes it's a specific EMS vendor based on whom they are working with. Sometimes we have an OEM that asks us to work with an EMS. trate design rules. The EMS vendors want to stay up to date on the latest and greatest technology, and we want to understand the issues in high volume manufacturing.

CA: Do material costs influence your choices?

CM: This is very important. What we have learned is that customers pay for "good enough." You basically have to meet their specification but you don't have to go beyond it. The other component is cost. Customers will buy a product with this size, performance, etc., at this given cost. Materials, especially in advanced packaging, are a significant part of the cost. We are looking at how we can improve yields so very little of the materials that are used get thrown away as part of the process. What is high cost today may not be high cost tomorrow. CSP was that way.

CA: Tessera has been on the forefront of SiP.

CM: We think packaging in general is a critical core to the miniaturization and integration of products. Miniaturization and integration are a balancing act at the system, board and packaging levels: You try to balance at the most effective way at each level. If you have integration at the chip level at a high yield, it can be the most cost-effective process. But you might have to decouple the two. Industry has invested billions upon billions of dollars, and there is great opportunity for packaging interconnects.

CA: Would you have predicted this when Tessera was launched?

CM: [Tessera cofounder] Tom DiStefano predicted circuitry coming off the chip and going into the substrate. And it makes sense. Take more of that surface routing and optimize it in the package instead. You wouldn't test the chip before

you packaged it because the package completed the circuit. I think in the next decade you will see more of that in reality.

CA: What will be the effect on known good die?

CM: I don't know if it will have a direct impact on KGD because you still need that. No single solution allows you to integrate all these. You need a 3-D toolbox. And in a 3-D toolbox you have multiple tools: through-silicon via, die stacking, package stacking. All these things are required to drive integration and miniaturization. If you look at the board and package assemblers, it will be having access to this toolkit that allows them to package the future.

CA: Does the move by certain EMS/ODMs into packaging complicate your relationship?

CM: There's been a migration of the package assemblers moving into board assembly, starting with module assembly. And the EMS guys are migrating into packaging. Flextronics and Foxconn have semiconductor packaging capability. And there will be some overlap. Each will need access to the other's capabilities. Does it complicate our relationship? No, because at the end of the day, our objective is to make technology broadly available, with more functionality, more performance, a better price point, and the right reliability.

<http://www.circuitsassembly.com/cms/component/content/article/159/9075-the-miniaturization-integration-balancing-act>