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Flip chip PoP is perfect for mobile, if done right

(November 10, 2010) -- [Package-on-package \(PoP\)](#), implemented with flip chip package assembly, is meeting a lot of the requirements for next-generation mobile devices. Challenges remain, namely using fine pitch underfill, brittleness of ultra low-*k* (ULK) dielectrics, and shorting between adjacent bumps. Craig Mitchell, Tesser, examines the lucrative [3D packaging](#) step and how to face the aforementioned challenges.

For years, the mobile phone market has been driving the development of the [advanced semiconductor packaging](#) industry. This is primarily due to the desire of original equipment manufacturers (OEMs) to accommodate the end user's insatiable demand for functionality, performance and miniaturized form factors. The mobile phone market's influence was first seen through the demand and subsequent adoption of [chip scale packaging \(CSP\)](#), followed closely by multi-chip packaging and now package-on-package (PoP) structures for manufacturing. This trend is most notable in the smart phone segment, where applications, baseband and multimedia processors are increasingly adopting flip chip packaging to satisfy size, performance, and, in some cases, cost requirements. The smart phone market is the fastest-growing segment of the 1.3-billion-unit mobile phone market, anticipated to grow at a CAGR of 25% through 2014, according to Gartner. It also tends to be the most profitable segment of the market and is gaining increased attention from wireless carriers, handset manufacturers, semiconductor manufacturers and subcontract assemblers alike.

The growing functionality and complexity of these handheld devices is driving the need for more advanced packaging interconnect technologies that are capable of efficiently and cost-effectively delivering the performance design to the chip and the end-product. Flip chip has been identified as a solution and, when combined with a PoP approach, is meeting many of the demands facing the semiconductor market. With that said, the global technical community still faces challenges in implementing flip chip, including fine pitch underfill, brittleness of ultra low-*k* (ULK) dielectrics and shorting between adjacent bumps. Here, we'll explore some of these challenges that are currently being considered.

The first challenge relates to [underfill](#), a widely used process in which a liquid material is dispensed to fill the gaps between the flip-chipped die and the associated package substrate. Its primary purpose is to reduce stress in the solder bumps interconnecting the die and the package substrate as a result of differences in coefficients of thermal expansion (CTE) and exposure to a range of temperatures through the lifetime of the package assembly. As the pitch of the flip chip bumps continues to decrease, it simply becomes more difficult to use conventional underfill processes and materials. Reduced bump pitch results in smaller gaps between adjacent flip chip bumps and lower stand-off height between the chip and the package substrate. Both result in increased resistance to the flow of the underfill material itself.

This, combined with the trend toward increased chip size, makes it increasingly difficult to ensure void-free, high-throughput underfill. Consequently, the industry is pursuing advanced encapsulation techniques such as capillary underfill, no-flow underfill, vacuum underfill and mold underfill, in addition to continually refining the rheology and various other mechanical and thermal properties of the underfill materials themselves. Although much progress has been made, further development of equipment, materials, and the associated processes is required.

Another challenge relates to the use of [ultra low-k dielectrics](#). As the wafer process node for manufacturing semiconductor devices migrates from micron to submicron to deep submicron levels, the need for thin, low-k insulative layers to separate and isolate adjacent on-chip conductors grows. At the 32nm process node and below, ULK dielectrics provide the required isolation while minimizing the parasitic capacitance to enable the desired switching speed within the semiconductor chip. To achieve the required dielectric constant of these insulating layers, voids are often introduced into the material, increasing its porosity. As air has a dielectric constant of one, introducing air into the dielectric is an effective means to decrease the dielectric constant. However, it can also substantially increase the material's brittleness, so it becomes critical to minimize stress on this fragile dielectric layer. Several solutions are being considered, including increasing top metal layers' thickness, increasing passivation layer thickness, and, in most if not all cases, very carefully selecting the underfill material to balance the mechanical properties, such as CTE and Young's modulus, with those of the ULK dielectric. **Also read**, ["Low-k family introduced by SBA Materials" by Dr. Phil Garrou](#)

A third challenge relates directly back to the flip chip interconnect itself and the requirement to have both fine pitch and sufficient stand-off height (typically, above 60µm) between the chip and the package substrate for underfill. For the past 40 years, [balls of solder](#), either tin/lead or lead-free, have been used as the primary flip chip interconnect. Reductions in bump pitch are pushing the limits of conventional assembly processes, resulting in lower substrate and package assembly yields, reduced manufacturing throughput and higher packaging costs. A common failure relates to electric shorting between adjacent solder bumps. This is due to the spherical nature of each solder mass, which results in roughly equal height and width of the solder mass. One solution is to take a more columnar approach, in which the height-to-width ratio is greater than one.

One approach that is gaining traction uses a copper column or pillar, either directly on the chip itself or on the package substrate. The [copper pillar approach](#) provides scalability to very fine pitch: 100µm-pitch area array. The columnar shape allows for taller stand-off height as well as greater gaps between adjacent contacts, eliminating shorting and reducing flow resistance to underfill, allowing for void-free underfill. Using a copper pillar on the package substrate in particular allows for solder, a lower modulus material than copper, to remain at the interface to the bond pad, helping address the ULK dielectric brittleness described earlier. **Also watch:** ["Leveraging 3D packaging technologies: Tessera shares its latest work"](#)

Conclusion

In summary, the demand for electronic products with higher functionality, higher performance, and smaller form factor is unlikely to abate anytime soon. The mobile phone market will continue to lead the charge, pushing the limits of advanced packaging technologies for years to come. With the number of connections to the chip growing, and the allowable package footprint shrinking, flip chip technology is increasingly employed for various processors in mobile handsets. Although conventional flip chip interconnect has proven sufficient for the

current generation of devices, new approaches, processes, materials, and structures will need to be developed to address the challenges of the future.



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