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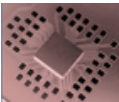
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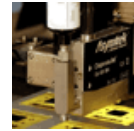


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Exclusive

December 3, 2009

Innovative High-Accuracy Wafer-Level Bonding Process

Abstract

With certain adjustments, the common technique of waferlevel bonding can solve one of the most critical issues in the semiconductor manufacturing process: alignment accuracy. An innovative bonding approach using a UVcurable adhesive allows the manufacturer to achieve lithography-scale resolutions.

Key Words: Through silicon via (TSV), wafer-level packaging, wafer-level camera module, alignment accuracy, wafer-level bonding



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Development Manager,
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1. Introduction

Wafer stacking is an important technique for the modern semiconductor industry, and aligned wafer bonding is used in several applications:

a. TSV integration

The most common use of this technology is to stack NAND Flash memory in a miniature multi-gigabyte unit used in Micro SD cards. To produce a thinner stack, the industry is moving from wire-bonding integration to the TSV method, in which the silicon chips can be integrated at the wafer level.(Fig.1) [1]

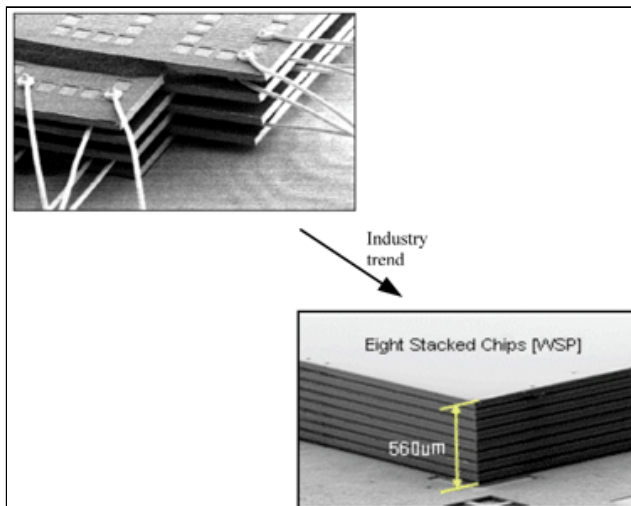


Fig. 1. Wire-bonded interconnection (left) is being replaced by the TSV stacking approach (right) using wafer-level bonding.

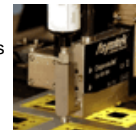
3-D Architectures for Semiconductor Integration and Packaging

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b. Wafer-level packaging

Tessera's SHELLCASETM wafer-level packaging solution for CMOS image sensors uses an aligned wafer-level bonding process for simultaneous encapsulation of the entire active surface of the imaging wafer. The optically transparent glass has patterned square features that seal the imaging area of each die, generating the air cavity above the imaging area (Fig. 2).

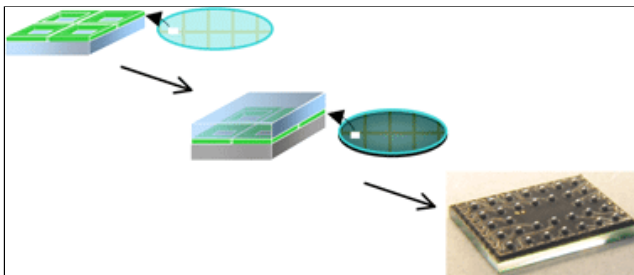


Fig. 2. The SHELLCASETM wafer-level packaging solution uses the aligned wafer-level bonding process to create the air cavity between the encapsulating glass and the imaging area.

c. Wafer-level camera module

In this application, several wafers with populated refractive optical elements are stacked together, producing a miniature multi-lens optical stack that is assembled on top of the packaged image sensor.

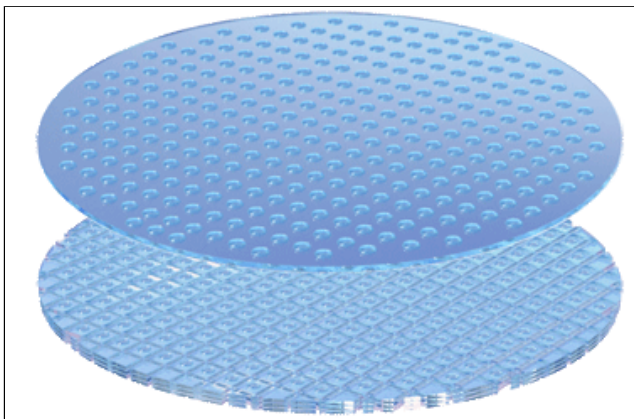


Fig. 3. Lenses are produced in a wafer form and stacked together using wafer-level bonding processes.

The following process flow is typical for most bonding equipment[2]:

1. Wafer preparation. One or both of the wafers are prepared differently depending on the bonding type:

- Adhesive bonding: Thermally cured adhesive is applied to one or both wafers using spray, spin or other technologies

Industry trend

- Intermetallic bonding: One of the substrates is patterned with indium deposited with a thin layer of gold or silver. The second wafer is patterned with a thicker gold or silver layer. The ratio of the metal thicknesses between the two wafers depends on the eutectic / intermetallic compound desired after bonding[3]

- Anodizing bonding: Two crystalline substrates, typically glass and silicon, are chemically treated and polished

- Plasma bonding: Both crystalline substrates, typically glass and silicon, are polished (patterned with silicon oxide, if required) and treated with oxygen plasma to generate high surface energy from the OH groups

2. Wafers are aligned using a tool such as an EVG 620 or a BA8. At the end of the aligning process, two wafers are clamped together in such a way that a gap of a few hundred microns is maintained between the two, due to the presence of three metal flags.

3. After clamping, the bonding chuck is dismantled from the aligner and installed into a bonding tool, such as an EVG 540 or an SB6e/8e, with two heated chucks with a web error compensation (WEC) mechanism inside the vacuum chamber. To prevent anodic bonding, the chucks are electrically connected to the power supply.

4. After the vacuum is generated, the top wafer is prefixed with a small pin in the center. The flags separating the two wafers face out from the cavity between the two wafers. Next, the wafers are brought into contact, and the top chuck generates the desired pressure to heat the chucks to the desired temperature.

The equipment cycle is illustrated in Figure 4.

This bonding approach involves several challenges:

1. Increasing the number of steps between alignment and bonding increases the risk of wafer movement. If one wafer moves during the chuck transfer, it can disrupt the position of the second wafer, separating the flags or interfering with the WEC process during bonding.

2. It can be difficult to ensure that bond-warped wafers are aligned precisely. During the alignment process in the aligner tool, the vacuum chucks flatten the wafers. After alignment, when the vacuum is released, the wafers may warp again, changing the wafers' pattern registration relative to each other. Once the top chuck of the bonding tool applies pressure, the wafers flatten out once more, but without any adjustments to the alignment. This problem causes post-bonding misalignment.

3. The bonding cycle is fairly slow, usually requiring up to 30 minutes. This has a significant effect on CAPEX in mass-production.

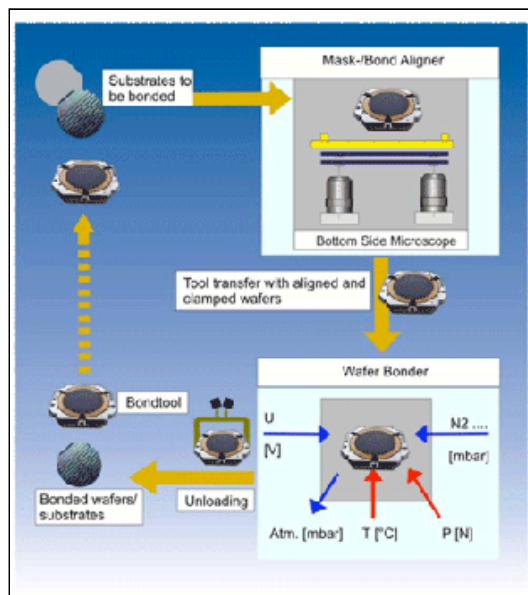


Fig. 4. Typical bonding cycle between alignment and bonding tools (EMC-3D SE Asia Technical Symposium, Jan. 22-26, 2007).

The manufacturing of wafer-level camera modules requires very precise alignment between the two lens wafers; much more precise than in other

applications, such as wafer-level packaging or TSV integration.

The following describes an innovative approach for bonding optical wafers with alignment accuracy similar to that achieved by the lithographic approach.

2. Experimental

Our work demonstrates the use of a UV adhesive (3553-UTF-HM epoxy) to bond two optical wafers. An advantage to this approach is that the wafers bond immediately after alignment, while still held in place by the vacuum chuck.

Our equipment setup uses an IQ Aligner. Our bonding process uses a nanoimprint lithography (NIL) setup, which is capable of large-gap alignment (Fig 5).

1. Our setup consists of two chucks. On top is a transparent vacuum chuck with a UV source above it.

Both chucks can move vertically, and the bottom chuck can move horizontally to align the two wafers on the X and Y axes

2. First, a transparent wafer is loaded on the bottom chuck. The wafer surface does not need to be 100% transparent; 50% transparency will be effective as well.

3. The bottom chuck lifts the wafer to the top vacuum chuck.

4. The bottom chuck returns to the load position.

5. The second wafer is coated with a UV adhesive and loaded onto the bottom chuck.

6. The bottom chuck brings the second wafer to a predefined distance from the first wafer, and the two wafers are aligned.

7. After alignment, the second wafer is brought into contact with the first wafer, and the stack is exposed to UV radiation through the top, transparent chuck.

8. Finally the bonded stack is unloaded from the system.

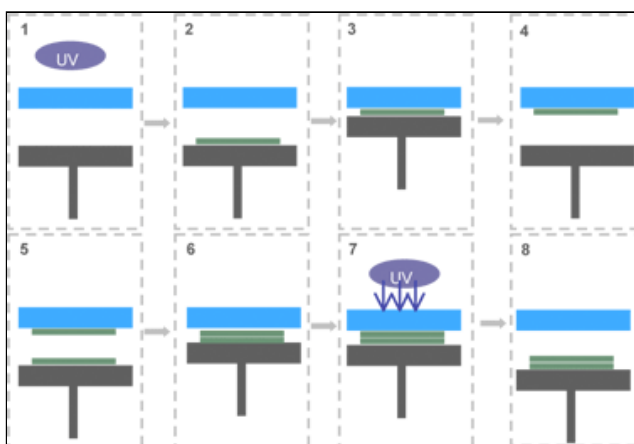


Fig. 5. Process flow using UV-sensitive adhesive as a bonding substance.

The alignment can be observed in real time (Fig. 6).

Since the adhesive is immediately cured by UV radiation after alignment, the wafers' relative registration cannot change.

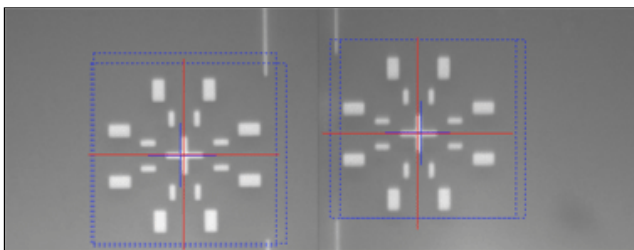


Fig 6. Relative registration of the alignment marks from the two wafers observed on the IQA aligner in real time.

3. Results

Data from the post-bonding alignment of the 11 bonded wafers are presented in Table 1 below. The alignment was measured on an UltraMet 100. Each stack was measured twice, from where the top wafer faces the UltraMet 100 chuck and where the bottom faces the chuck.

Wafer #	Measurements	XL	XR	YL	YR
1	Wafer 1 up	-3.16	3.32	-0.23	-1.87
		-3.08	3.25	-0.18	-1.91
	Wafer 2 up	-3.00	3.45	-0.02	-2.37
2	Wafer 1 up	-2.99	3.44	-0.03	-2.26
		-2.53	2.97	0.69	-2.61
	Wafer 2 up	-2.55	3.07	0.54	-2.65
3	Wafer 1 up	-2.53	2.99	0.91	-3.02
		-2.50	3.05	0.91	-2.98
	Wafer 2 up	-3.05	2.84	2.54	1.40
4	Wafer 1 up	-3.24	2.63	2.68	1.59
		-3.39	2.98	3.10	1.19
	Wafer 2 up	-3.09	3.10	3.46	1.35
5	Wafer 1 up	-3.22	4.13	3.19	2.23
		-3.02	3.79	3.45	2.30
	Wafer 2 up	-2.62	3.85	3.97	2.74
6	Wafer 1 up	-2.92	3.70	3.73	2.28
		-1.80	4.26	2.38	0.35
	Wafer 2 up	-1.69	4.28	2.50	0.39
7	Wafer 1 up	-1.76	4.22	2.68	0.75
		-1.70	4.18	2.69	0.57
	Wafer 2 up	-3.24	3.00	2.10	-0.60
8	Wafer 1 up	-3.25	2.98	2.19	-0.50
		-3.17	2.79	2.42	-0.62
	Wafer 2 up	-3.13	2.85	2.43	0.59
9	Wafer 1 up	-2.20	3.87	1.11	-0.35
		-2.18	3.97	1.09	-0.36
	Wafer 2 up	-2.22	3.84	1.45	-0.18
10	Wafer 1 up	-2.16	3.92	1.41	-0.13
		-2.92	3.02	3.47	3.72
	Wafer 2 up	-2.92	3.02	3.72	3.47
11	Wafer 1 up	-2.70	2.90	4.12	3.69
		-2.66	2.85	4.11	3.67
	Wafer 2 up	-2.70	3.53	1.11	-0.39
12	Wafer 1 up	-2.94	2.63	-0.45	-0.75
		-2.85	3.44	1.76	-0.78
	Wafer 2 up	-3.33	3.55	1.58	-0.55
13	Wafer 1 up	-2.55	2.91	2.20	-0.09
		-2.26	2.79	2.36	-0.21
	Wafer 2 up	-2.58	3.20	3.30	-0.03
14	Wafer 1 up	-2.56	3.15	3.36	-0.06
		-2.91	2.46	3.71	1.73
	Wafer 2 up	-2.68	2.38	3.68	1.59
15	Wafer 2 up	-2.38	2.51	3.65	1.36
		-2.43	2.35	3.69	1.24

Table 1. Row alignment data for wafer-to-wafer bonding.

Our results are presented in Table 2. Note that these numbers are very close to the lithography spec, since we performed the bonding process on a tool with NIL capabilities.

	XL	XR	YL	YR
Average	0.36	0.36	2.28	1.44
Total Sigma	0.36	0.36	1.26	1.13
Sigma meas.	0.20	0.20	0.55	0.48
Average + 3 sigma (not including the sigma measurements)	1.27	1.27	5.67	4.52

Table 2. Statistical analysis of the row data.

Source

Alignment accuracy is strongly correlated with optical performance, as shown in Figure 7, which depicts sample MTF plots of poorly and properly aligned optics. In the properly aligned examples, the MTF curves of the different field-of-view angles overlap sufficiently, providing higher MTF values on a sufficiently wide FFL window. In the poorly aligned optics, the curves are split.

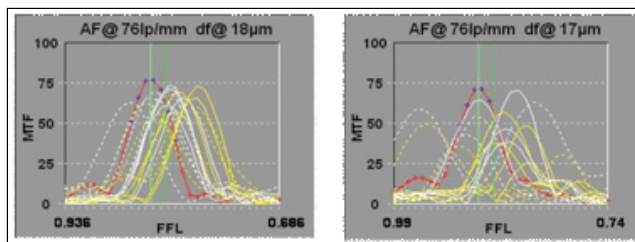


Fig 7. The MTF plot of properly (left) and poorly (right) aligned optics.

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[1] "Market trend for 3D stacking", Yole Developpement, EMC 3D, June 2007, p. 5.

[2] EMC-3D SE Asia Technical Symposium, Jan. 22-26, 2007.

[3] "Low Temperature Eutectic Bonding

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