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Raised Copper Contact Technologies for IC Packaging-A Path to Improved Reliability

By Joe Fjelstad

Interconnections are arguably the most critical element in electronic system design, and deservedly they are presently getting much greater attention than they have had in the past. Interconnections are found at every level from the chip to the system, and they are also normally the weak link. Nearly every electronic failure can be traced to a point of interconnection. Most commonly, the failure is found in a solder joint, and such failures have been on the rise since the legislatively forced adoption of lead-free solder based on the EU's well intended but completely misguided RoHS legislation. One of the good things that comes with every problem is the opportunity learn and hopefully to make things better. In that regard, the EU's lead-free mandate has proven to be a treasure trove of learning opportunities, and there have been some clever responses to the technical challenges that have accompanied its introduction.

While most of attention has been focused on soldering of components to printed circuit boards successfully and the reliably challenges associate with such efforts, soldering at the level of the chip package (i.e., flip chip assembly) creates a similar but substantively different set of challenges to assure reliable products. The solutions that have garnered the most attention in this regard are those that cluster around the basic concept of providing a raised copper contact on either the chip or the substrate. Of these, the creation of copper contacts on the chip is most common. Depending on how one defines a copper standoff, these types of solutions could trace their roots back to the origins of flip chip transistors, where copper balls were soldered to the chips to provide a gap between the chip and the substrate. In the late 1980s and 1990s, copper bumping of wafers was explored, culminating in wafer level packages being produced by Fujitsu and Casio, the die thereon having copper posts which were electroformed in place by plating into cylindrical cavities. Because the resulting copper contacts resembled small copper posts, the image gave rise to their descriptive name. While copper posts offer improvement over some of the other bump and solder ball solutions, their performance is less than optimum. This topic will be covered later in a comparison of test results between competing solutions.

In contrast to copper posts developed in Japan, another solution has been developed by scientists and engineers at Tessera in San Jose, CA. Tessera's solution addresses the problem from the

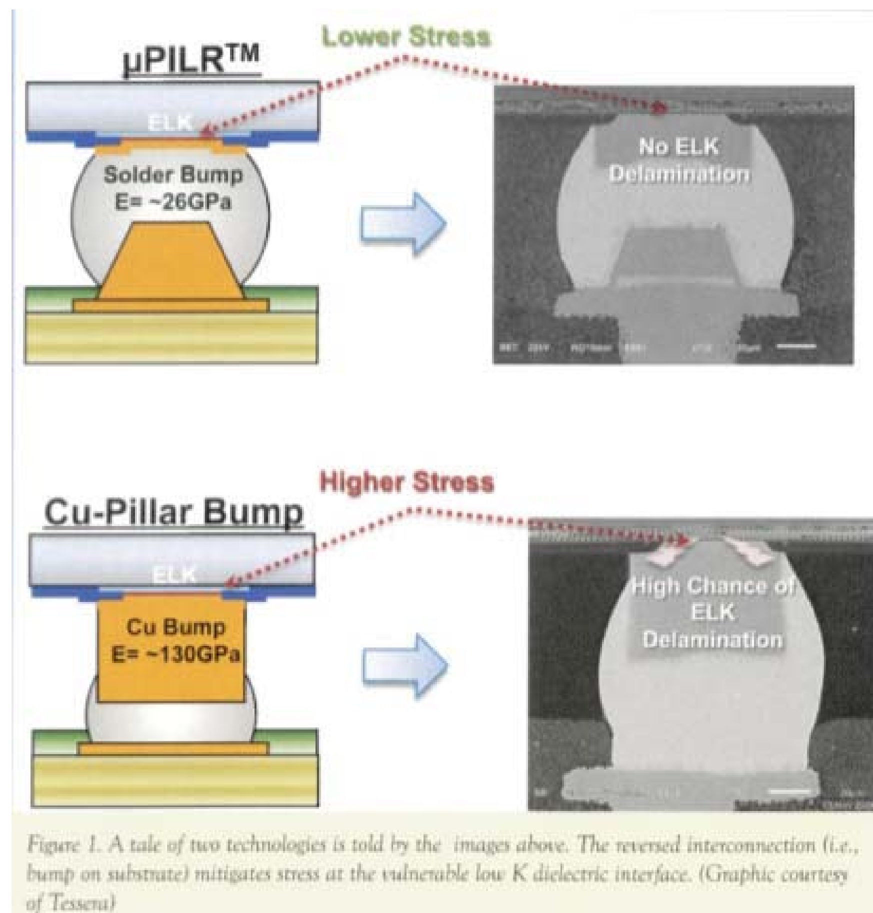

Figure 1. A tale of two technologies is told by the images above. The reversed interconnection (i.e., bump on substrate) mitigates stress at the vulnerable low K dielectric interface. (Graphic courtesy of Tessera)

opposite side by providing copper pillars (a term of distinction first introduced and used by the company and owing to the difference in processing and the unique look of the completed copper contacts) on the substrate rather than the chip. The results of taking such an unconventional approach are impressive, but then the company built its reputation on unconventional solutions that have solved fundamental challenges facing the electronics industry. A prime example is the company's world renowned µBGA® (micro BGA) IC packaging solution, which dominates the IC memory space.

Tessera's µPILR™ technology was first discussed in this column as a concept that was then in development. Now with the data on test results available, the story is even more compelling. One of the advantages of the Tessera solution, as was mentioned before, is that the contacts are extremely planar, a result of the contacts being etched from a sheet of precision-rolled copper foil. This helps to assure that all contacts on a flip chip (or IC package) will have a near perfect mating contact resulting in improved assembly yield. The solution also allows for the highest standoff and best post height-to-width aspect ratio, which makes it a very attractive choice for fine pitch assembly.

The structure also appears to obviate the types of cracks that are commonly seen with standard solder ball attach. This is increasingly important as IC designers opt to use brittle low K dielectrics. This is illustrated in Figure 1. The graphical comparison's suggestion is substantiated by test data that provide evidence of the structure's benefit both in thermal cycling and in the arguably more important drop test. The drop test is highlighted because it has proven to be the "Achilles Heel" of lead-free soldering and a common failure mechanism for packaged devices mounted to substrates. That aside, thermal cycling remains an important benchmark test. In a thermal cycle test comparing copper post on chip to the µPILR contact used in a flip chip package (18 x 16.68 mm flip chip die on 45 x 45 mm substrate), the data indicate a 50% improvement for thermals cycling. For the drop testing, which is a package-level concern, a 12 x 12 mm package-on-package with 0.4 mm pitch on the bottom IC package and 0.5 mm pitch on top package, both employing the µPILR copper pin concept, the data show a very impressive 8x improvement of the µPILR compared to a traditional solder ball. Those interested in reviewing more of the data, including Weibull charts, should contact Tessera's technical marketing department.

In summary, the use of copper pin-like structures offers significant benefit to improving product life both at chip and package level. Given the inherent problems with lead free solder, solutions such as the one developed by Tessera should see increased use by manufactures concerned about the rising cost of product returns due to poor reliability, premature failure and, perhaps most important, the attendant loss of customer confidence.

Verdant Electronics founder and president Joseph (Joe) Fjelstad has more than 35 years of international experience in electronic interconnection and packaging technology in a variety of capacities from chemist to process engineer and from international consultant to CEO. Mr. Fjelstad is also a well known author writing on the subject of electronic interconnection technologies. Prior to founding Verdant, Mr. Fjelstad co-founded SiliconPipe a leader in the development of high speed interconnection technologies. He was also formerly with Tessera Technologies, a global leader in chip-scale packaging, where he was appointed to the first corporate fellowship for his innovations.

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