

Novel and Low Cost Through Silicon Via Solution for Wafer Scale Packaging of Image Sensors

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Abstract- Solid state image sensors are being incorporated in an every increasing diversity of products. Typically each year more than 1 billion image sensors are produced, which primarily find application in portable electronics products such as camera 'phones, digital still cameras and increasingly, laptop computers. Predictions are that this market will continue growing for some years as cell phones with multiple cameras become the norm and automotive driver aids enter the video age, which could entail 10 or more cameras being installed on each vehicle. Consumer demand for vast quantities of camera modules at very low price is forcing a search for new packaging technologies utilising radically different materials.

Key to packaging image sensors in high volume with good yields and at low cost is wafer scale processing. In wafer scale processes a large number of die are packaged simultaneously, so satisfying the manufacturing volume requirement, while the costs are shared among the good die on the wafer, making it economically compelling compared with discrete packaging. The protection provided by the package ensures high camera yields.

Image sensors have to be installed face-up wards so the optically active area is presented to the scene of interest. Connection of the die bond pads to the package ball grid array (BGA) interface requires some form of through silicon via (TSV). However, TSVs are traditionally very expensive to fabricate and have a poor reputation for reliability.

This paper will present a new TSV solution suitable for both single die and stacked die wafer-scale packages. So-called 'via-through-pad' interconnects are a novel form of interconnect that superficially resemble a TSV but the differences are important and have profound implications for the product cost and reliability. Unusually, the materials of

the package construction are sourced from outside the semiconductor industry. This is done to keep costs as low as possible. The process technology is wholly scaleable so the same tool set can be used irrespective of the wafer diameter. Data will be presented showing via-through-pad interconnects are able to surpass by a wide margin, the exacting reliability requirements of the automotive industry, both at the package and board level.

I. INTRODUCTION

Solid state image sensors are extremely delicate components. Not only do they suffer from the normal failure mechanisms of conventional CMOS devices, but the optically active area is easily damaged. Even a wash with de-ionised water can have catastrophic consequences. Similarly, if a particle of dirt as small as 1 μ m diameter, which is 100 times less than the width of a human hair, lands on the sensor it will cause a highly visible black spot in the image. In order to meet reliability specifications, image sensors must be packaged in a way that protects them from the environment, without affecting the optical performance. For these reasons, the very first step of a wafer scale image sensor packaging process is to attach a cover glass to the face of the image sensor wafer.

The cover glass is not attached to the entire face of the image sensor wafer. Instead, it is attached by a picture frame seal of adhesive that surrounds the optical area on each die and spaces the glass cover about 40 μ m from micro lens array that covers the imaging area. Sawing the assembly yields individual die, each with an optically transparent cover over the delicate image sensor area. This process is illustrated schematically in Fig. 1.



Fig. 1 Formation of a wafer level cavity package. Left - the device wafer containing five image sensors. Middle - application of the seal material to form a picture frame around the perimeter of each die. Right - attachment of a lid material to seal the cavity over each die with an air space between the device wafer and the cover glass. Singulation frees the packaged die from the wafer. Source: Tessera.

II. THROUGH SILICON VIA INTERCONNECTS

One challenge of wafer level packaging of image sensors is making contact to the bond pads, which are on the front face of the die and inaccessible underneath the glass cover that protects the optically active area of the die. One solution is through silicon via (TSV) technology. There are many variations of TSVs, a common implementation being a hollow pipe, with near-vertical sidewalls, machined through the thickness of the silicon. Onto the sidewalls of the pipe is applied a dielectric film overlaid with conductive metal. The via is machined by deep reactive ion etching using the Bosch process[1].

Despite being technically possible for many years, TSVs have never been adopted in high volume manufacture. There are several reasons for this notable amongst which is the high capital cost of the equipment required, the slow etch rate of silicon, which curtails throughput, and the complexity of the additional process steps to fabricate conductive vias that are insulated from the silicon through which they pass. There are also issues of reliability that have not yet been satisfactorily solved. Points of weaknesses in the design include dielectric and conductive coating of the side walls of a high aspect ratio pipe; the 90 degree bends at the top and base of the pipe that the redistribution layer (RDL) must traverse and maintain connectivity during thermal cycling; and the difficulty of cleaning the back of the bond pad so the RDL can make an Ohmic contact, when it is the bottom of a long narrow pipe. A further consideration is that because the TSVs extend through the entire thickness of the die it is impossible to place any semiconductor circuitry in the region of the bond pads. A decrease in silicon utilization results in an increase in die size and a direct impact on the component price.

A modern wafer level package for image sensors is shown in Fig. 2. In this design connection between the bond pads and the ball grid array is by a via-through-pad technology. This solution means there are few restrictions on the bond pad size, pitch or location, making it directly compatible with the majority of existing CMOS imagers. The dicing lanes can be as narrow as the silicon design rules allow, which helps to maximize the number of die per wafer and decrease unit cost. The packaged imager thickness is approximately 500 μm , making it imminently

suitable for electronics products where the current fashion is for extreme thinness.

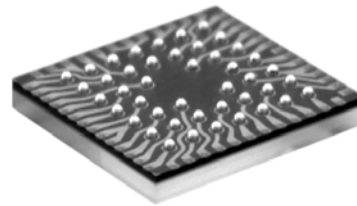


Fig. 2 Image sensor packaged at the wafer level and provided with a ball grid array (BGA) interface to simplify and cheapen attachment to a printed circuit board. Connection between the die bond pads and the wiring trace attached to the BGA is achieved by a novel through silicon via (TSV) solution based on via-through-pad technology. Source: Tessera.

The via-through-pad interconnect superficially resembles a TSV but the differences are important and have profound implications for the product cost and reliability. In this contact the RDL penetrates through the thickness of the bond pad to form a circumferential edge contact. This is structurally similar to the well established edge contact and hence has the same inherent reliability. Because the act of penetrating the bond pad exposes fresh metal at the circumference this solution obviates the difficulty of making Ohmic contact between the RDL and the bond pad.

Via-through-pad interconnects require passageway through the silicon wafer. However, unlike TSVs, the opening is purely mechanical and needs only to expose sufficient area of the bond pad to permit formation of the via-through-pad edge contact. Consequently the alignment accuracy and limits on pitch can be relaxed since several interconnects can share a single opening. Because the openings through the silicon do not have to be individual, the profile of the openings can be relaxed to a trapezoid with rounded corners. This eliminates one of the sources of unreliability of TSVs. Finally, because via-through-pad interconnect is based on polymer technology with a single redistribution layer for the wiring trace, it is very cost-effective compared with other wafer level packaging solutions.

III. ELECTROPHORETIC MATERIALS

One of the main costs of wafer level packages is the materials set. Traditional semiconductor materials are too expensive for a

product where the ultimate goal is a video graphics array (VGA) camera module priced at under \$1. A solution was identified in the form of a product already used in high tonnage by the automotive industry. Electrophoretic paints are materials that are deposited using the principle of electrostatic attraction. An electrocoat system applies a direct current charge to a metal part immersed in a bath of oppositely charged paint particles (see Fig. 3). The paint particles are drawn to the metal part and adhere to it forming an even, continuous, film over every surface and in every crevice and corner, until the coating reaches the desired thickness. At that thickness, the film insulates the part so attraction stops and electrocoating is complete. The thickness is controlled by the voltage applied to the electrocoat bath and typically ranges from 5-75 μ m. Electrophoretic paints were developed to improve the corrosion resistance of car bodies with added benefit of excellent colour and gloss control compared with sprayed paints. They do not contain heavy metals, generate little or no hazardous air pollutants and liberate very low levels of volatile organic chemicals. Bake temperatures are typically around 120°C. Above all, they are very low cost and some grades of electrophoretic paint can endow steel parts with corrosion resistance in excess of two thousand salt spray hours.

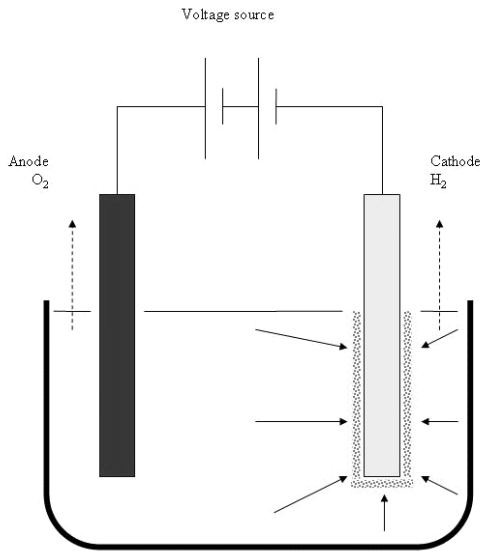


Fig. 3 Principle elements of a cathodic electrocoating system. The part to be coated is immersed in a bath and forms the cathode electrode in a circuit to which the electrophoretic paint is attracted. Gas evolution occurs from both the anode and cathode as a by product of the coating process. Source: Tessera.

Data sheets for electrophoretic paints attest that they can only be applied to metals because the whole of the part to be coated must form either a cathode or anode in the electrochemical cell. Fortunately, because electrophoretic materials are potential rather than current driven, it was found that semiconductor grade silicon possesses sufficient electrical conductivity to allow direct coating, greatly simplifying the process flow. A second attribute of the electrophoretic paints being electric field dependent is that the deposit laterally spreads beyond the conductor, allowing small gaps of insulator to be bridged.

The material[2] selected for this application is an epoxy, resin-based system that contains 23% solids by weight. This product is not a dangerous preparation according to directive 1999/45/EC. Application is by a cathodic system. In the final design a single layer of electrophoretic paint is applied, about 15 μ m thick.

IV. RELIABILITY

Components intended for integration into products must be fit for purpose. The objective of the study was to develop an image sensor package suitable not just for portable electronics products, but able to meet the far more exacting automotive environment.

For semiconductor parts the necessary tests are defined by Standards. The principal package- and board-level tests and accompanying environmental parameters for automotive applications are summarised in Tables I and II.

A typical test sample comprises a minimum of 3 lots of 77 parts taken from production batches manufactured on different days by different shifts on the full range of equipment available. The parts developed in this project exhibit a margin of safety of more than two and often substantially more[3] over the required reliability Standards as shown by the results presented in Table III.

Table I. Reliability Standard for Imagers Destined for Automotive Applications

Conditions and Duration	Test and Standard
125 +5/-0 °C, 24hrs 85 +/-20 °C; 85 +/-5% RH, 168hrs Gradient <30 °C/sec 100-150 °C for 60-120sec 183 °C for 60-150 sec 265 +0/ -5 °C for 10-30 sec Gradient <6 °C/sec	Preconditioning – moisture soak level one (MSL1) JESD22-A113-D

Time from 25 °C to peak <8 min x 3 cycles	
85 +5/-0 °C 85 +/-2 °C; 60 +/-3% RH 2000 hrs	Temperature and humidity after MSL 1 JESD22-A101-B
150 +/-5 °C 2000 hrs	High temperature storage after MSL 1 JESD22-A103-A
Min: -40 +0/-10 °C ; Max: 125 +15/-0 °C 32 cycles/ day 2000 cycles	Thermal cycling after MSL 1 JESD22-A104-B

Table II. Automotive Board Level Specification Environmental Tests for Microelectronic Components

Readout points	Conditions	Test
Completion	3x lead-free reflow cycles	Preconditioning
1,000hrs pass/fail	150°C	High temperature storage
1,000hrs pass/fail	-40°C	Low temperature storage
168hrs pass/fail	85°C, 85%RH	Damp heat storage
168hrs pass/fail	121°C, 100%RH, 2atm	Autoclave
1,000cyc pass/fail	-40°C to 125°C, 10min dwell, <7sec transition	Thermal shock
1,000cyc pass/fail	-30°C to 125°C, 30min dwell, <1min transition	Thermal cycling
Completion	30x 1.5m all faces on to concrete	Free fall drop
1,500g, 2,000g and 2,500g pass/fail	5x all 6 axes	Mechanical shock
Completion	20 to 2000 Hz, 8gs, 15 mins, each direction	Variable frequency vibration

Table III. First Failure on Environmental Testing of Solid State Imagers in Wafer Level Packages having Novel Through Silicon Vias and Sealed with Electrophoretic Paint.

Test	First failure detection
Temperature and humidity	4688 hrs (2.3 x specification)
High temperature storage	4307 hrs (2.2 x specification)
Thermal cycling	4450 cycles (2.2 x specification)

V. CONCLUSIONS

The very large number of solid state cameras required for modern electronics products means that new manufacturing methods are necessary to meet production rate and cost targets. Presented is a new wafer-level chip size packaging technology compatible with automotive requirements. In this technology the image sensor is protected from contamination using a cover glass from the initial stage of processing. The electrical contacts are then routed to the back side of the silicon to a ball grid array interface by a novel through silicon via solution. The

package is suitable for standard surface mount assembly. Being a true wafer level chip size technology the packaged die is of the same size as the original die. The thickness of the packaged die is significantly reduced in this technology, thus decreasing the camera module size. In addition, the package economics benefit from the shared costs of wafer level processing.

Sealing of the image sensor package by electrophoretic paint enables the parts to achieve high reliability, making this packaging solution the technology of choice for image sensors in portable electronics and automotive applications.

REFERENCES

- (1) F. Laermer and A. Schilp, "Method of Anisotropically Etching Silicon", US patent No. 5,501,893, 1996
- (2) Powercron 645 manufactured by PPG (UK) Ltd.
- (3) G. Humpston, L. Mirkarimi, and M. Huynh, "Board Level Reliability of Solid State Camera Modules", Proceedings IMAPS 40th International Symposium on Microelectronics, San Jose, 13-14 November 2007