

Optical Performance of Bare Image Sensor Die and Sensors Packaged at the Wafer Level and Protected by a Cover Glass

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ABSTRACT

The yield of solid state camera modules declines with increasing imager resolution. The easiest means of compensating for this trend is to package the imager die before they are assembled into camera modules. The packaging is preferably accomplished at the wafer level. The package cover is a sheet of glass that forms part of the optical train of the solid state camera. This paper discusses the properties required of the glass and describes a computer model that was constructed to provide quantitative insight into its effect on the optical performance of image sensors. The study corroborates practical measurements that the cover glass has no significant effect on the low light sensitivity of a typical camera module. The cover glass does introduce some reflection losses and minor image aberrations, but these can be managed through the combination of attention to the design of the total optical path and making the cover glass as thin as possible.

Key words: Solid state imager, wafer-level package, cover glass, optical model

INTRODUCTION

Solid state image sensors are manufactured in vast quantities. Typically each year more than 1 billion image sensors are produced, which primarily find application in portable electronics products such as camera 'phones, digital still cameras and increasingly, laptop computers. Predictions are that this market will continue growing for some years as cell phones with multiple cameras become the norm and automotive driver aids enter the video age, which could entail 10 or more cameras being installed on each vehicle.

PACKAGING OF SOLID STATE IMAGERS

In common with most other semiconductor devices, solid state image sensors require some form of enclosure in order to ensure their longevity. Traditionally for imagers this was achieved using chip-on-board (COB) assembly processes. In this scheme the imager is attached to a substrate and wire bonds form interconnections between bond pads on the die and lands on the substrate. The substrate forms the base of the enclosure. Over the die is then placed a lens turret, which houses the optical train of the camera. The lens turret is sealed to the substrate so the lower optical surface in combination with the sidewalls of the turret form an enclosure for the die. This is illustrated in Figure 1.

This structure has two principal drawbacks. The first is that the cost of assembly is incremental for each die packaged. A second limitation is that the imager die is totally unprotected until the final assembly operation when the lens turret is attached. It is therefore not surprising that more than 90% of defects in camera modules are related to contamination by particles¹. The short-term solution is to invest in clean rooms and operator training. However, many solid state camera module manufacturers are already operating Class 10 environments, or better, so there is not a great deal of scope for further improvement at affordable cost.

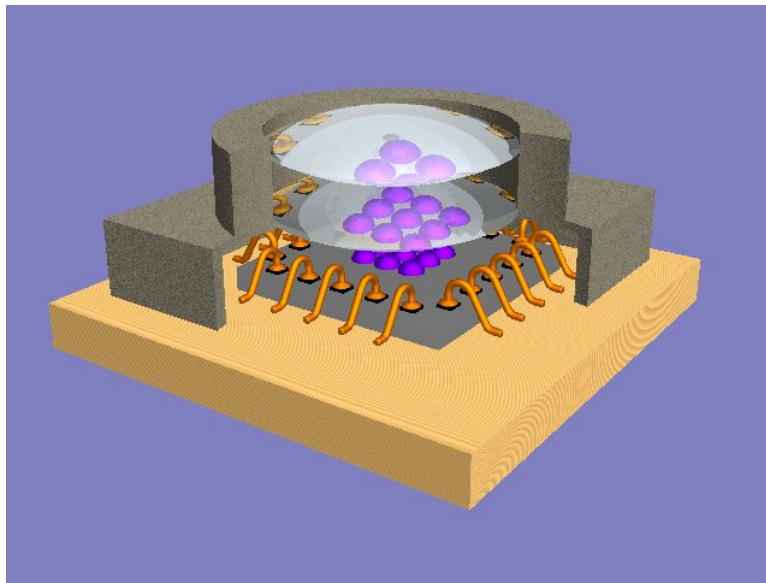


Fig 1 Camera module assembled using chip-on-board processes. The lens turret housing forms a seal over the exposed die. Drawing not to scale. Source: Tessera

WAFER LEVEL PACKAGING

Wafer-level packaging (WLP) is an alternative approach where the die are packaged while still in wafer form and the wafer is then singulated to free individually packaged die. WLP has the advantage that the costs of packaging are shared among the good die on the wafer, greatly reducing packaging costs per die. A wafer-level cavity package for an image sensor is achieved simply by applying a picture frame of adhesive around each die, attaching a glass wafer and then sawing the assembly to yield individual die, each with a cover over the delicate image sensor area. This process is illustrated schematically in Figure 2.

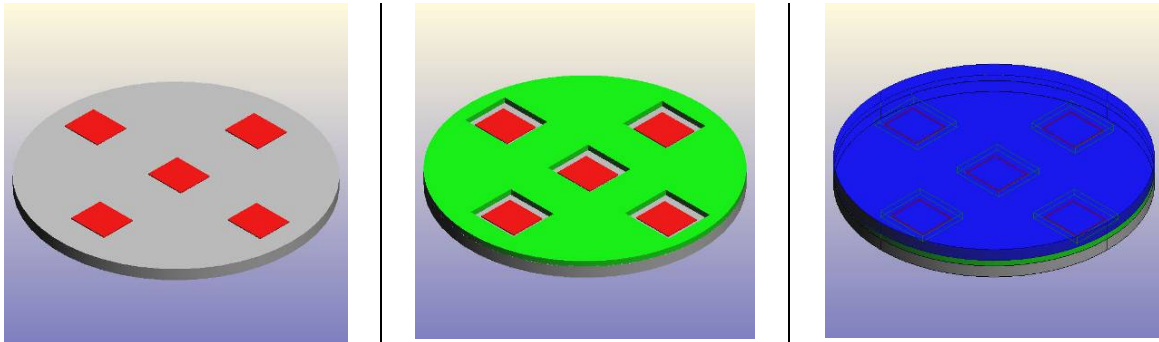


Fig 2 Formation of a wafer-level cavity package. Left - the device wafer containing five die. Middle - application of the seal material to form a picture frame around the perimeter of each die. Right – attachment of a lid material to seal the cavity over each die. Singulation frees the packaged die from the wafer, an example of which is shown in Figure 3. Source: Tessera

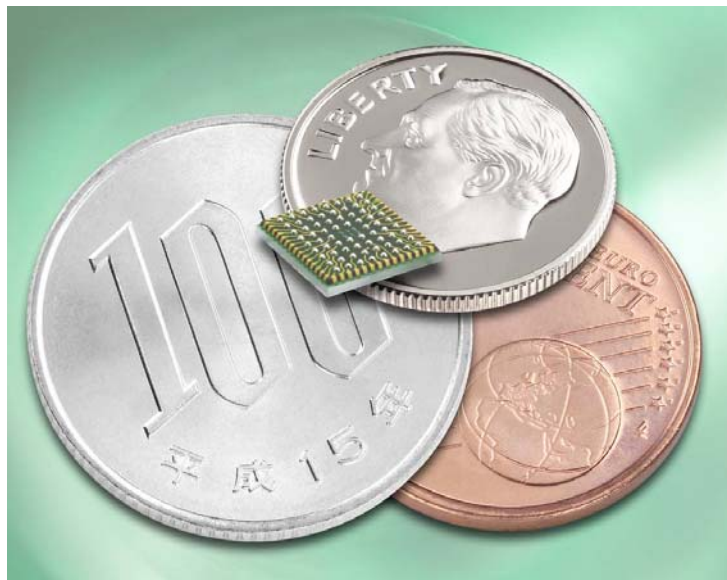


Fig 3 Image sensor packaged at the wafer level² and provided with a ball grid array interface to simplify and cheapen attachment to a printed circuit board. Source: Tessera

Wafer-level packaging provides two benefits that have great value for image sensors. Firstly, the dies are protected from the very first step of the assembly process so that yield loss from contamination is minimized. The second benefit is that it is possible to provide the packaged die with a ball grid array interface. This permits the camera module to be soldered to the main printed circuit board of the product at the same time as all the other semiconductor and passive components. It is predicted that by 2010 more than half of all image sensors will be protected by wafer-level packages.

COVER GLASS

The cover glass used for the wafer-level package must fulfil several criteria. These are:

- Optically transparent. The glass must allow incident radiation of the visible spectrum (400-700nm) to reach the image sensor. The through thickness transparency of the cover glass needs to be as high as possible since any attenuation has a direct bearing on the low light sensitivity of the camera.
- Reasonably closely matched in thermal expansivity to silicon over the temperature range -40°C to +260°C. To benefit from the economics of wafer-level processing, the cover glass is bonded to the silicon die while both are in wafer form. This means that the expansivity of the glass must be closely matched to silicon above room temperature since joining of the glass to silicon entails an elevated temperature process.
- Free of active species that could potentially leach out of the glass and degrade the delicate image sensor. In this regard, the elements normally found in glass that are particularly detrimental are the alkalis. Over time these can leach out of the glass and poison the semiconductor junctions.
- Be available in wafer form, to match the diameter and features of SEMI standard silicon wafers (e.g. flats, notches). Similarly, the glass wafers must be manufacturable to exacting specifications in terms of defects, since most types of blemish in the glass will be visible as artefacts in the image captured by the sensor. A typical scratch/dig specification for image sensor cover glass is 50/05. In addition, the geometric properties such as thickness and total thickness variation (TTV) need to be well controlled.
- Cost attractiveness. The packaging market is driven by challenging price roadmaps, thus high costs for materials and components are not acceptable. A major cost driver in the production of glass wafers is the polishing step. Choosing a hot forming method for the raw glass production that offers the desired thickness directly from the tank saves the expensive polishing step.

COVER GLASS SELECTION

There are very few glass types that meet the requirements set out above. The one selected for this application has the designation SCHOTT AF 45³. Its properties and performance are proven to meet the requirements for 200mm manufacturing lines in mass production for several years. In order to provide a suitable glass type for 300mm production lines as well as single glass WLP solutions, the glass type with the designation SCHOTT AF 32⁴ has been developed.

AF 45 as well as AF 32 are melted using selected pure raw materials. This ensures the high luminous transmittance in the visible wavelength, as can be seen from Figure 4.

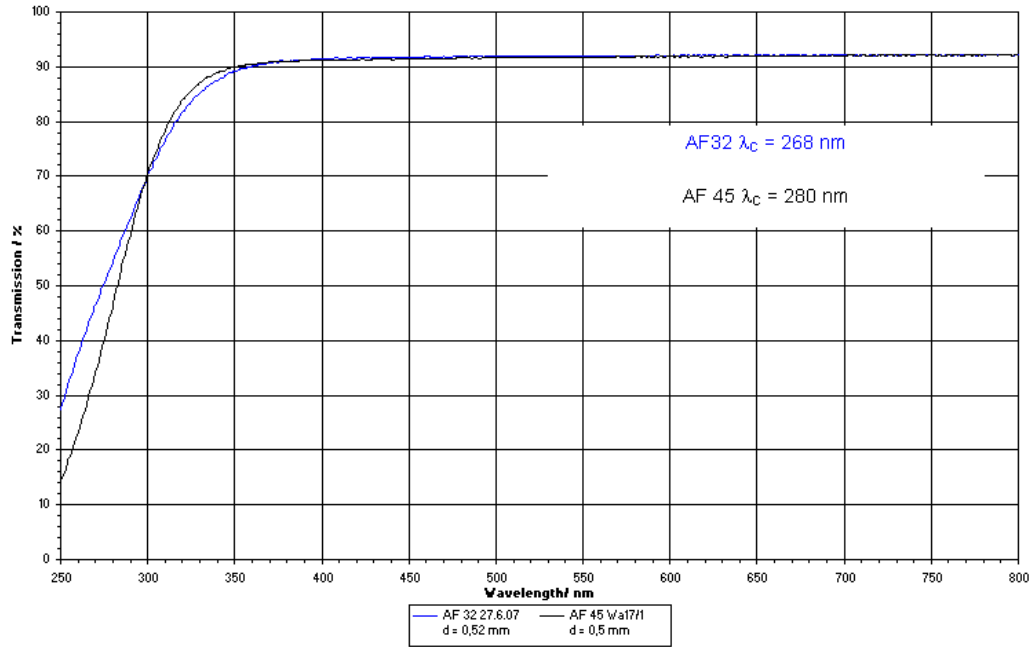


Fig. 4 Transmission of AF 45 and AF 32 as a function of wavelength. Source Schott AG

The most important difference between the two glass types is the lower coefficient of thermal expansion (CTE) of AF 32 which has a very close match to the CTE of silicon, as can be seen in Figure 5. As a result the bond between the cover glass and the silicon is very flat even for wafer sizes of 300mm diameter.

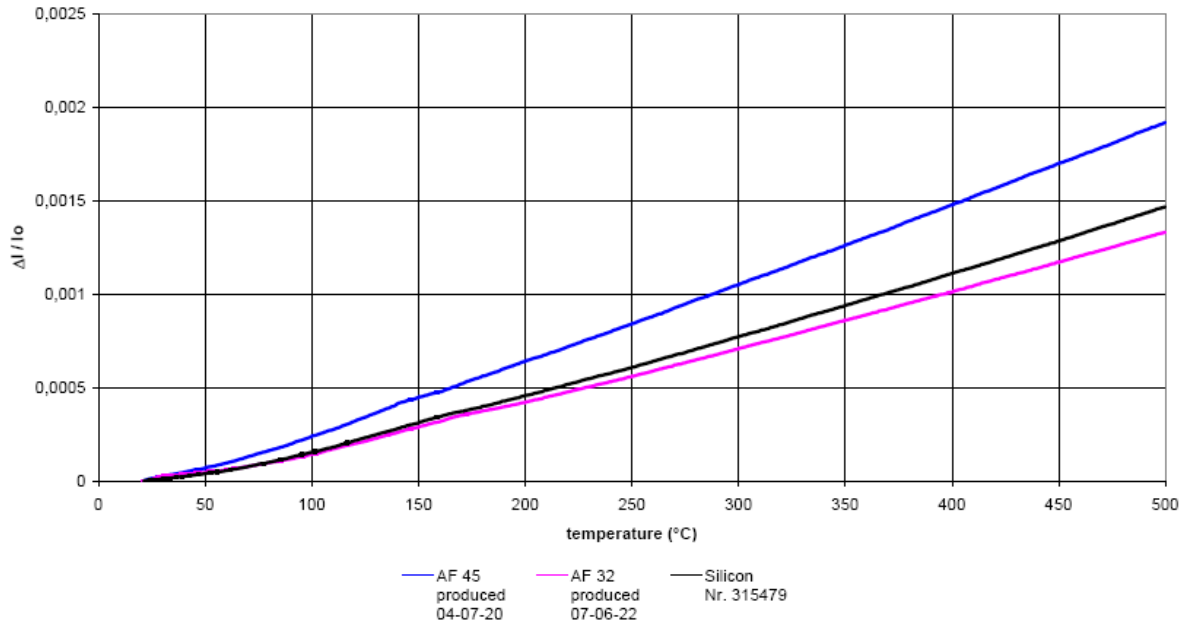


Fig 5 Dynamic elongation in initial length $\Delta l/l_0$ with a heat-up rate of 5K/min of AF 32, AF 45, and silicon. Source Schott AG.

The two glass types AF 45 and AF 32 are free of alkalis, which is indicated by the AF (Alkali Free) in the glass name. The glass compositions do not intentionally contain any oxides of lithium, sodium or potassium.

Both AF 45 and AF 32 are easy to process into the required wafer format. Table 1, below, shows an example of typical wafer specifications that can be achieved when choosing the above mentioned glass types.

Requirement	Specification	Tolerance
Size (diameter/square)	50 – 300mm	± 0.1mm
Thickness	0.1 – 1.1mm	± 10µm - ± 15µm
TTV	standard: +/- 10µm	advanced: +/- 5µm
Roughness	standard: ≤ 1 nm	
Cleaning	Ultra Sonic (US) and Mega Sonic (MS) in clean room class 1000	
Surface defects (scratch/dig)	standard: 10/5	advanced: 5/1
Packaging	wafer boxes or equivalent	
Structuring	holes and cavities possible	

Table 1 SCHOTT AF32 and AF45 wafer specifications and tolerances. Source Schott AG

Both AF 45 and AF 32 are manufactured by the down-draw process which enables the production of many different thicknesses in the range of 0.1mm up to 1.1mm at a TTV of +/- 10µm as a standard. Compared to other hot forming technologies, down-draw tanks are relatively small thus the transition cost from one thickness to the other is not as high for float glasses. The many available standard thicknesses as well as the relatively low minimum order quantity for customized thicknesses eliminate the need for the expensive mechanical polishing process. Beside the fact that down-drawn glasses come in the right thickness they have a very smooth surface with a roughness of below 1nm RMS, which is more than adequate for a cover glass on a camera module package.

OPTICAL PERFORMANCE

A key determinant of whether a camera module is suitable for a particular application is its optical performance. A camera module fabricated using COB assembly and one built using an imager protected by a WLP differ in one key regard, namely that the component packaged at the wafer level has a cover glass as an additional element in the optical path. The objective of this work was to evaluate the effect of the cover glass on the optical performance of miniaturized camera modules, typified by the type of device commonly employed in camera ‘phones, using a combination of experimental techniques and numerical simulation.

EXPERIMENTAL TECHNIQUE

The test vehicle was a CMOS imager of 1.3 Mpixel resolution, with a pixel dimension of 3.3µm. The imager was married to test station optics that gave a field of view diagonal between -1.0 and +1.0 coordinates i.e. 81 degrees horizontal and 59 degrees vertical. The photosensitive area illumination efficiency (PAIE) was measured for each pixel colour (red, green and blue), resolved to 8 bits, with different cover glass thicknesses of 300, 400 or 500µm. Variation in PAIE between different imagers from the same wafer was also measured.

RESULTS OF THE EXPERIMENTS AND DISCUSSION

The measured PAIE per pixel colour for different cover glass thicknesses is given in Figure 6. Two conclusions can be drawn from the data. As expected, the PAIE is highest in the centre of the image area and decreases toward the periphery, decreasing abruptly beyond the field of view. By normalising the PAIE measurements relative to the 300 μm cover glass it can be seen that the PAIE is reduced for each colour as the cover glass increases in thickness, as can be seen in Table 2. The magnitude of the trend is placed in context by measuring multiple die from the same wafer, each with a 500 μm thick cover glass. Normalising the results to the first die, the fluctuations of PAIE for other die, presented in Table 3, show clearly that the die-to-die performance variation on a given wafer is at least of the same magnitude, if not larger than the impact of the cover glass thickness.

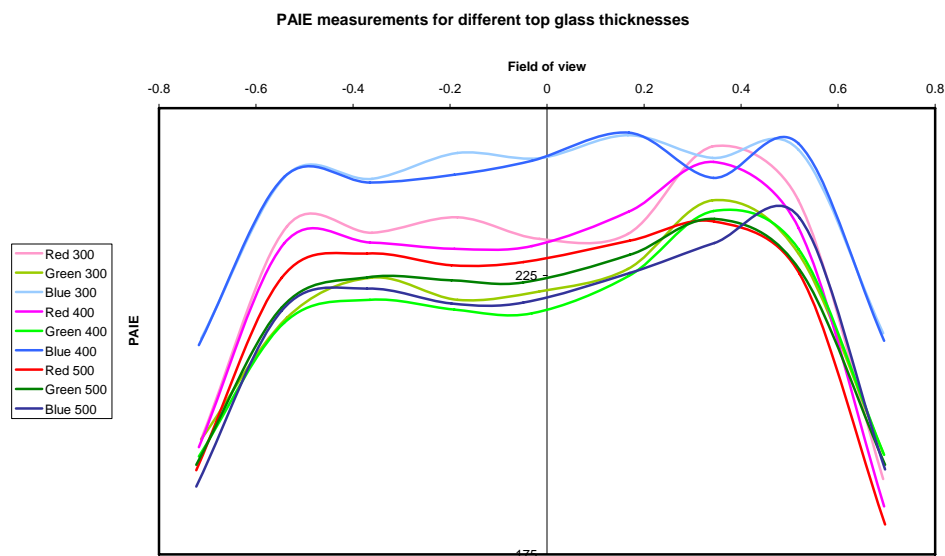


Fig 6 Measured PAIE per pixel colour for different cover glass thicknesses. Source: Tessera.

	Glass 300 microns	Glass 400 microns	Glass 500 microns
Red coloured pixels	100%	98.9%	96.7%
Green coloured pixels	100%	99.2%	99.8%
Blue coloured pixels	100%	99.5%	90.6%
AVERAGE	100%	99.2%	95.7%

Table 2 Measured PAIE per pixel colour normalized for a cover glass thickness of 300 μm . Source: Tessera.

	Min. fluctuation die-to-die	Average fluctuation of die-to-die	Max. fluctuation of die-to-die
Red coloured pixels	0.9%	2.3%	4.6%
Green coloured pixels	-2.5%	-0.6%	1.6%
Blue coloured pixels	5.1%	9.9%	13.6%

Table 3 Measured PAIE per pixel colour for multiple die from the same wafer, with 500 μm thick cover glass, normalized to the first die measured. Source: Tessera.

The results of the experiment imply the cover glass has no significant impact on the optical performance of the image sensor. However the difficulty of making accurate measurements, plus the die-to-die variation encountered suggested numerical modelling of the optical system might be a worthwhile alternative approach.

NUMERICAL SIMULATION

The objective of the numerical simulation was to analyse the optical performance of a solid state camera module, with and without a cover glass over the imager, via PAIE and crosstalk calculations. To do this a computer model (ZEMAX) was constructed to perform the required non-sequential ray trace simulation.

The imaged object was a 0.28mm x 0.28mm square surface located 100mm from the imaging lens. The source emits unpolarized light at 510nm. The object was a diffuse cosine source with distribution:

$$I(\theta) \approx I_0 \times \cos(\theta)^{C_n}$$

where $C_n = 10,000$ such that the illumination is hyper-Lambertian, namely a narrow lobe with rotationally symmetric distribution about the optical propagation axis.

The lens is a 50mm double-Gauss wide field of view lens with an effective focal length of 5.8mm. The lens field of view is 46° and the simulations were carried out at three fields of view: 0° , 13.4° and 20° . The lens f-number ($f\#$) was varied between 1.2, 2.0 and 4.0 by changing the diameter of the lens entrance pupil.

The CMOS device was reduced to a resolution of 5x5 pixels to decrease the computation time. A larger array would not add further insight as all of the optical phenomena of interest are already present in this low resolution device. The pixel size is $3.3\mu\text{m}$.

On top of the CMOS imager was constructed a 5x5 micro lens array, built from toroid lenses. The lenses have a flat back face, $2.0\mu\text{m}$ thickness and identical radius of $2.37\mu\text{m}$ on both curvatures.

Where present, the cover glass is $300\mu\text{m}$ thick and spaced $40\mu\text{m}$ from the front face of the CMOS imager to mimic the real life wafer-level package. The insertion of the AF45 glass plate to the system introduces a focal shift of $0.142 \pm 0.01\text{mm}$. This is expected and was accounted for in the simulation by shifting the CMOS imager to the new focal plane.

Simulating the optical behaviour of the camera was carried out in two steps. First, a sequential ray trace was used to locate the image plane of the double-Gauss lens for each field angle and f-number used. The criteria used for optimization was minimum spot size. Next, the CMOS imager with micro lens array was added and a non-sequential ray trace was performed with the source object inserted 100mm in front of the lens. The elements were positioned such that the imaging lens was focused on the photodiode layer. A detector object was placed on the back side of the photodiode layer with dimensions: $0.02 \times 0.02\text{mm}$ and 128×128 pixels. A Monte Carlo ray trace with 200,000 rays was run and the incoherent intensity of all rays hitting the detector plane recorded. The total power and peak irradiance were then derived. The performance of the model was assumed adequate when the resulting image resolved the discrete 5×5 pixel array. Such an image indicates that the micro lens array is functioning and the illumination is concentrated on the pixels.

PAIE is defined as the normalized, integrated intensity of the active pixels. Calculation of this parameter was as follows:

- a) Non-sequential calculation of the intensity image using Monte-Carlo simulation.
- b) The diffraction spot of the system was calculated from the point spread function for each F-number (1.2, 2.0 and 4.0).
- c) Both intensity image and diffraction spot were convoluted.

- d) A binary 2-D grid corresponding to the pixel dimension (pitch, size) and fill factor (40%) was generated.
- e) The grid and convoluted image were multiplied.

The PAIE is the ratio of the integrated image from step (e) and the convoluted image, step (d).

The pixel crosstalk is calculated using the following scheme using diffraction-limited paraxial optics instead of the double-Gauss lens. This is in order to eliminate aberrations due to the imaging lens:

- a) The diffraction spot is calculated via the point spread function of a single micro lens + CMOS layers.
- b) An intensity image is simulated with a Monte-Carlo run. However, unlike the previous case, a point source was used and the beam was focused on a single pixel in the micro lens array.
- c) Both images were convoluted and multiplied by the 2D grid as in the PAIE routine.
- d) The intensity of each of the central, illuminated pixel and the nearest 8 pixels is summed.
- e) The XT is defined using the following two methods:
 - The ratio of the highest neighboring pixel and the illuminated pixel (XT_{MAX}).
 - The ratio of all 8 neighboring pixels and the illuminated pixel (XT_{TOT}).

RESULTS OF THE NUMERICAL SIMULATION AND DISCUSSION

Table 4 gives the total power and peak irradiance calculated at the detector plane following non-sequential tracing of 200,000 rays for a COB imager and one in a wafer level package. Table 5 gives the calculated PAIE and XT_{MAX} and XT_{TOT} for the same two package styles.

Package	Field	Total Power (W)	Peak Intensity (W/cm ²)
COB	0.00	0.253	7.59E+05
COB	0.67	0.164	7.16E+05
COB	1.00	0.091	5.78E+05
WLP with Schott AF 45	0.00	0.223	7.02E+05
WLP with Schott AF 45	0.67	0.143	6.48E+05
WLP with Schott AF 45	1.00	0.081	5.09E+05
<i>Comparative results</i>			
COB vs. WLP	0.00	11.9%	7.6%
COB vs. WLP	0.67	12.7%	9.5%
COB vs. WLP	1.00	11.1%	11.9%

Table 4 Total power and peak irradiance at the detector plane (200,000 rays). Source: Tessera.

Package	field	F#	PAIE	XT _{MAX} [%]	XT _{TOT} [%]
COB	0.00	1.20	0.654	2.22	7.90
COB	0.67	1.20	0.589		
COB	1.00	1.20	0.600		
COB	0.00	2.00	0.673	2.05	7.33
COB	0.67	2.00	0.659		
COB	1.00	2.00	0.666		
COB	0.00	4.00	0.674	2.05	7.33
COB	0.67	4.00	0.660		
COB	1.00	4.00	0.666		

WLP with Schott AF 45	0.00	1.20	0.662	3.15	10.80
WLP with Schott AF 45	0.67	1.20	0.595		
WLP with Schott AF 45	1.00	1.20	0.579		
WLP with Schott AF 45	0.00	2.00	0.683	2.38	8.46
WLP with Schott AF 45	0.67	2.00	0.622		
WLP with Schott AF 45	1.00	2.00	0.592		
WLP with Schott AF 45	0.00	4.00	0.683	2.32	8.25
WLP with Schott AF 45	0.67	4.00	0.638		
WLP with Schott AF 45	1.00	4.00	0.607		

Table 5 PAIE and XT for camera modules with and without a cover glass over the image sensor die. Source: Tessera.

Under ideal conditions, the only difference between the two package configurations should be reflection and absorption losses due to the cover glass. These effects will be most noticeable at large field angles. The AF45 glass has an index of 1.53 at 0.5 μ m and thus a reflection loss of about 9% is expected. The measured differences in the total power between amount to approximately 12% (Table 4) and are within the experimental error of these simulations, as some light is lost due to scattering from surfaces. However, as shown in Table 6, the difference in PAIE values is small, amounting to about 3% when averaging over all field angles and F-numbers. This value is also small compared with the measurements reported above for die-to-die variations within a single wafer.

	COB	WLP
<i>mean</i>	0.649	0.629
<i>Std dev</i>	0.032	0.040

Table 6 Overall PAIE comparison between imagers with and without cover glass. Source: Tessera.

It should be noted that PAIE represents the efficiency of the system and therefore the reflection losses shown in Table 4 are cancelled out in the PAIE calculation. Crosstalk values are slightly lower for the COB imager since the AF45 cover glass adds some noise to the system. This could be compensated for by thinning the glass. Both methods of XT calculation result in similar ratios for the two cases. Crosstalk is generally more sensitive to added surfaces in the vicinity of the surface plane than to surfaces further out, implying that a taller cavity package is preferable whenever permitted.

CONCLUSIONS

Packaging of image sensors at the wafer level is becoming essential as resolutions increase and pixel dimensions decrease. While this is technically tractable and economically favourable a packaged image sensor must have a cover glass as an additional component in the optical train. The cover glass has to meet very exacting specifications but suitable products are commercially available nevertheless. The effect of the cover glass on the optical performance of the camera has been measured experimentally and analysed by numerical simulation. The cover glass has negligible effect on the low light sensitivity of the camera module because its transmittance is so high. As expected, the cover glass introduces reflection losses and some minor image aberrations. The reflection losses can be managed by designing the optical system to function at low chief ray angles while the aberrations are minimized by making the cover glass as thin as possible.

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